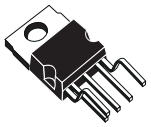
VIPer20/SP/DIP
VIPer20A/ASP/ADIP

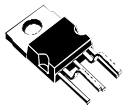
SMPS PRIMARY I.C.

TYPE	V_{DSS}	I_n	$R_{DS(on)}$
VIPer20/SP/DIP	620V	0.5 A	16 Ω
VIPer20A/ASP/ADIP	700V	0.5 A	18 Ω

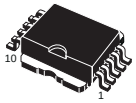
- ADJUSTABLE SWITCHING FREQUENCY UP TO 200 kHz
- CURRENT MODE CONTROL
- SOFT START AND SHUT DOWN CONTROL
- AUTOMATIC BURST MODE OPERATION IN STAND-BY CONDITION ABLE TO MEET "BLUE ANGEL" NORM (<1W TOTAL POWER CONSUMPTION)
- INTERNALLY TRIMMED ZENER REFERENCE
- UNDERVOLTAGE LOCK-OUT WITH HYSTERESIS
- INTEGRATED START-UP SUPPLY
- AVALANCHE RUGGED
- OVERTEMPERATURE PROTECTION
- LOW STAND-BY CURRENT
- ADJUSTABLE CURRENT LIMITATION



PENTAWATT HV



PENTAWATT HV (022Y)



PowerSO-10™

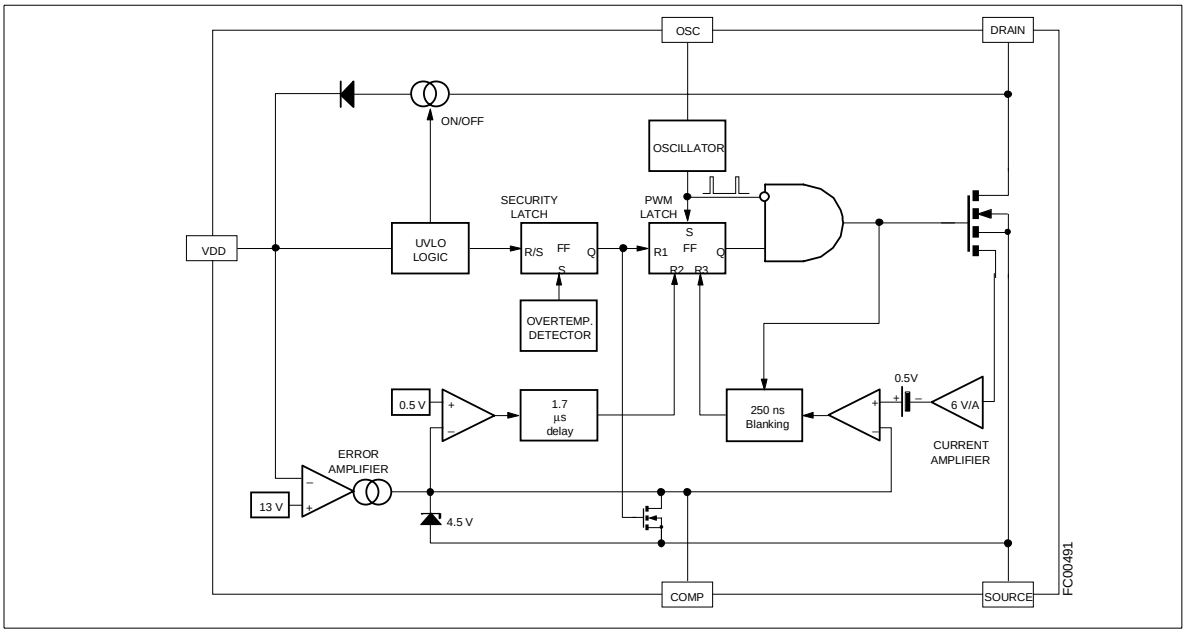
DIP-8

DESCRIPTION

VIPer20/20A, made using VIPower M0 Technology, combines on the same silicon chip a state-of-the-art PWM circuit together with an optimized high voltage avalanche rugged Vertical Power MOSFET (620V or 700V / 0.5A).

Typical applications cover off line power supplies with a secondary power capability of 10W in wide range condition and 20W in single range or with doubler configuration. It is compatible from both primary or secondary regulation loop despite using around 50% less components when compared with a discrete solution. Burst mode operation is an additional feature of this device, offering the possibility to operate in stand-by mode without extra components.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DS}	Continuous Drain-Source Voltage (T_j=25 to 125°C) for **VIPer20/SP/DIP** for **VIPer20A/ASP/ADIP**	 -0.3 to 620 -0.3 to 700	 V V
I_D	Maximum Current	Internally limited	A
V_{DD}	Supply Voltage	0 to 15	V
V_{OSC}	Voltage Range Input	0 to V_{DD}	V
V_{COMP}	Voltage Range Input	0 to 5	V
I_{COMP}	Maximum Continuous Current	± 2	mA
V_{esd}	Electrostatic Discharge (R =1.5kΩ; C=100pF)	4000	V
$I_{D(AR)}$	Avalanche Drain-Source Current, Repetitive or Not Repetitive (T_C=100°C; Pulse width limited by T_j max; δ < 1%) for **VIPer20/SP/DIP** for **VIPer20A/ASP/ADIP**	 0.5 0.4	 A A
P_{tot}	Power Dissipation at T_c=25ºC	57	W
T_j	Junction Operating Temperature	Internally limited	°C
T_{stg}	Storage Temperature	-65 to 150	°C

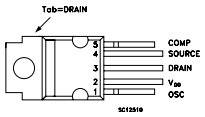
THERMAL DATA

Symbol	Parameter		PENTAWATT	PowerSO-10™ (*)	DIP-8	Unit
$R_{thj\text{-}pin}$	Thermal Resistance Junction-pin	Max			20	°C/W
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.0	2.0		°C/W
$R_{thj\text{-}amb.}$	Thermal Resistance Ambient-case	Max	70	60	35 (#)	°C/W

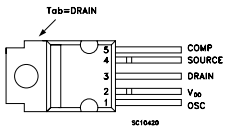
(*) When mounted using the minimum recommended pad size on FR-4 board.
(#) On multylayer PCB.

CONNECTION DIAGRAMS (Top View)

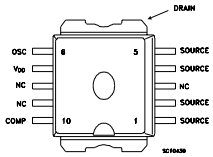
PENTAWATT HV



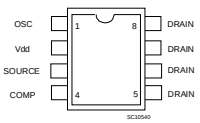
PENTAWATT HV (022Y)



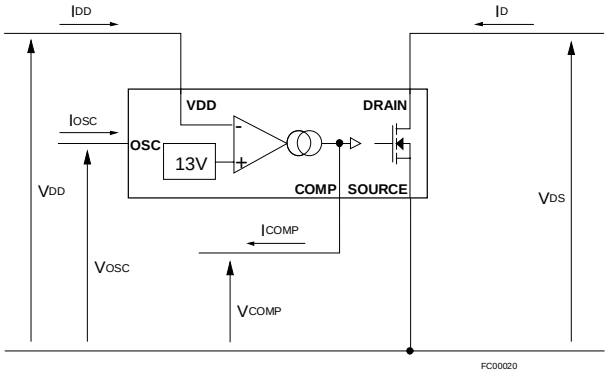
PowerSO-10™



DIP-8



CURRENT AND VOLTAGE CONVENTIONS



ORDERING NUMBERS

PENTAWATT HV	PENTAWATT HV (022Y)	PowerSO-10™	DIP-8
VIPer20	VIPer20 (022Y)	VIPer20SP	VIPer20DIP
VIPer20A	VIPer20A (022Y)	VIPer20ASP	VIPer20ADIP

PINS FUNCTIONAL DESCRIPTION

DRAIN PIN:

Integrated Power MOSFET drain pin. It provides internal bias current during start-up via an integrated high voltage current source which is switched off during normal operation. The device is able to handle an unclamped current during its normal operation, assuring self protection against voltage surges, PCB stray inductance, and allowing a snubberless operation for low output power.

SOURCE Pin:

Power MOSFET source pin. Primary side circuit common ground connection.

VDD Pin:

This pin provides two functions:

- It corresponds to the low voltage supply of the control part of the circuit. If V_{DD} goes below 8V, the start-up current source is activated and the output power MOSFET is switched off until the V_{DD} voltage reaches 11V. During this phase, the internal current consumption is reduced, the V_{DD} pin sources a current of about 2mA and the COMP pin is shorted to ground. After that, the current source is shut down, and the device tries to start up by switching again.

- This pin is also connected to the error amplifier, in order to allow primary as well as secondary regulation configurations. In case of primary regulation, an internal 13V trimmed reference voltage is used to maintain V_{DD} at 13V. For secondary regulation, a voltage between 8.5V and 12.5V will be put on V_{DD} pin by transformer design, in order to stick the output of the transconductance amplifier to the high state. The COMP pin behaves as a constant current source, and can easily be connected to the output of an optocoupler. Note that any overvoltage due to regulation loop failure is still detected by the error amplifier through the V_{DD} voltage, which cannot overpass 13V. The output voltage will be somewhat higher than the nominal one, but still under control.

COMP PIN:

This pin provides two functions:

- It is the output of the error transconductance amplifier, and allows for the connection of a compensation network to provide the desired transfer function of the regulation loop. Its bandwidth can easily be adjusted to the needed value with usual components value. As stated above, secondary regulation configurations are also implemented through the COMP pin.

- When the COMP voltage goes below 0.5V, the shut-down of the circuit occurs, with a zero duty cycle for the power MOSFET. This feature can be used to switch off the converter, and is automatically activated by the regulation loop (whatever is the configuration) to provide a burst mode operation in case of negligible output power or open load condition.

OSC PIN:

An R_t-C_t network must be connected on that pin to define the switching frequency. Note that despite the connection of R_t to V_{DD}, no significant frequency change occurs for V_{DD} varying from 8V to 15V. It also provides a synchronization capability, when connected to an external frequency source.

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
$I_{D(AR)}$	Avalanche Current, Repetitive or Not Repetitive (pulse widht limited by T_j max; $\delta < 1\%$) for **VIPer20/SP/DIP** for **VIPer20A/ASP/ADIP** (see fig.12)	 0.5 0.4	 A A
$E_{(ar)}$	Single Pulse Avalanche Energy (starting T_j =25ºC, $I_D=I_{D(ar)}$) (see fig.12)	10	mJ

ELECTRICAL CHARACTERISTICS (T_j=25°C; V_{DD}=13V, unless otherwise specified)

POWER SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Voltage	I_D=1mA; V_{COMP}=0V for **VIPer20/SP/DIP** for **VIPer20A/ASP/ADIP** (see fig.5)	 620 700			 V V
I_{DSS}	Off-State Drain Current	V_{COMP}=0V; T_j=125°C V_{DS}=620V for **VIPer20/SP/DIP** V_{DS}=700V for **VIPer20A/ASP/ADIP**			 1.0 1.0	 mA mA
$R_{DS(on)}$	Static Drain-Source On Resistance	I_D=0.4A for **VIPer20/SP/DIP** for **VIPer20A/ASP/ADIP** I_D=0.4A; T_j=100°C for **VIPer20/SP/DIP** for **VIPer20A/ASP/ADIP**		 13.5 15.5	 16 18 29 32	 Ω Ω Ω Ω
t_f	Fall Time	I_D=0.2A; V_{IN}=300V (1) (See fig. 3)		100		ns
t_r	Rise Time	I_D=.4A; V_{IN}=300V (1) (See fig. 3)		50		ns
C_{oss}	Output Capacitance	V_{DS}=25V		90		pF

(1) On Inductive Load, Clamped.

SUPPLY SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DDch}	Start-Up Charging Current	V_{DD}=5V; V_{DS}=35V (see fig. 2 and fig. 15)		-2		mA
I_{DD0}	Operating Supply Current	V_{DD}=12V; F_{SW}=0kHz (see fig. 2)		12	16	mA
I_{DD1}	Operating Supply Current	V_{DD}=12V; F_{sw}=100kHz		13		mA
I_{DD2}	Operating Supply Current	V_{DD}=12V; F_{sw}=200kHz		14		mA
V_{DDoff}	Undervoltage Shutdown	(See fig. 2)	7.5	8	9	V
V_{DDon}	Undervoltage Reset	(See fig. 2)		11	12	V
V_{DDhyst}	Hysteresis Start-up	(See fig. 2)	2.4	3		V

ELECTRICAL CHARACTERISTICS (continued)

OSCILLATOR SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SW}	Oscillator Frequency Total Variation	R_t=8.2KΩ; C_t=2.4nF V_{DD}=9 to 15V; with R_t± 1%; C_t± 5% (see fig. 6 and fig. 9)	90	100	110	kHz
V_{OSCih}	Oscillator Peak Voltage			7.1		V
V_{OSCil}	Oscillator Valley Voltage			3.7		V

ERROR AMPLIFIER SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{DDreg}	V_{DD} Regulation Point	I_{COMP}=0mA (see fig. 1)	12.6	13	13.4	V
ΔV_{DDreg}	Total Variation	T_j=0 to 100°C		2		%
G_{BW}	Unity Gain Bandwidth	From Input =V_{DD} to Output = V_{COMP} COMP pin is open (see fig. 10)		150		kHz
A_{VOL}	Open Loop Voltage Gain	COMP pin is open (see fig. 10)	45	52		dB
G_m	DC Transconductance	V_{COMP}=2.5V (see fig. 1)	1.1	1.5	1.9	mA/V
V_{COMPLO}	Output Low Level	I_{COMP}= -400µA; V_{DD}=14V		0.2		V
V_{COMPHI}	Output High Level	I_{COMP}=400µA; V_{DD}=12V		4.5		V
I_{COMPLO}	Output Low Current Capability	V_{COMP}=2.5V; V_{DD}=14V		-600		µA
I_{COMPHI}	Output High Current Capability	V_{COMP}=2.5V; V_{DD}=12V		600		µA

PWM COMPARATOR SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
H_{ID}	ΔV_{COMP} / ΔI_{DPEAK}	V_{COMP}=1 to 3 V	4.2	6	7.8	V/A
$V_{COMPoff}$	V_{COMP} Offset	I_{DPEAK}=10mA		0.5		V
I_{Dpeak}	Peak Current Limitation	V_{DD}=12V; COMP pin open	0.5	0.67	0.9	A
t_d	Current Sense Delay to Turn-Off	I_D=1A		250		ns
t_b	Blanking Time			250	360	ns
$t_{on(min)}$	Minimum On Time			350		ns

SHUTDOWN AND OVERTEMPERATURE SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{COMPth}	Restart Threshold	(see fig. 4)		0.5		V
t_{DISsu}	Disable Set Up Time	(see fig. 4)		1.7	5	µs
T_{tsd}	Thermal Shutdown Temperature	(See fig. 8)	140	170	190	°C
T_{hyst}	Thermal Shutdown Hysteresis	(See fig. 8)		40		°C