Not recommended for new designs – Please use 93LC76C or 93LC86C.

93LC76/86

8K/16K 2.5V Microwire Serial EEPROM

Features:

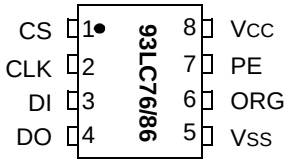
- Single Supply with Programming Operation down to 2.5V
- Low-Power CMOS Technology
  - 1 mA active current typical
  - 5 μA standby current (typical) at 3.0V
- ORG Pin Selectable Memory Configuration
  1024 x 8 or 512 x 16-Bit Organization (93LC76)
  2048 x 8 or 1024 x 16-Bit Organization (93LC86)
- Self-Timed Erase and Write Cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power On/Off Data Protection Circuitry
- Industry Standard 3-Wire Serial I/O
- Device Status Signal during Erase/Write Cycles
- Sequential Read Function
- 1,000,000 Erase/Write Cycles Ensured
- Data Retention > 200 years
- 8-Pin PDIP/SOIC Package
- Temperature Ranges Available
  - Commercial (C) 0°C to +70°C
  - Industrial (I) -40°C to +85°C

Description:

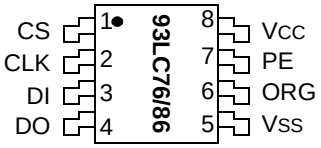
The Microchip Technology Inc. 93LC76/86 are 8K and 16K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power nonvolatile memory applications. These devices also have a Program Enable (PE) pin to allow the user to write-protect the entire contents of the memory array. The 93LC76/86 is available in standard 8-pin PDIP and 8-pin surface mount SOIC packages.

Package Types

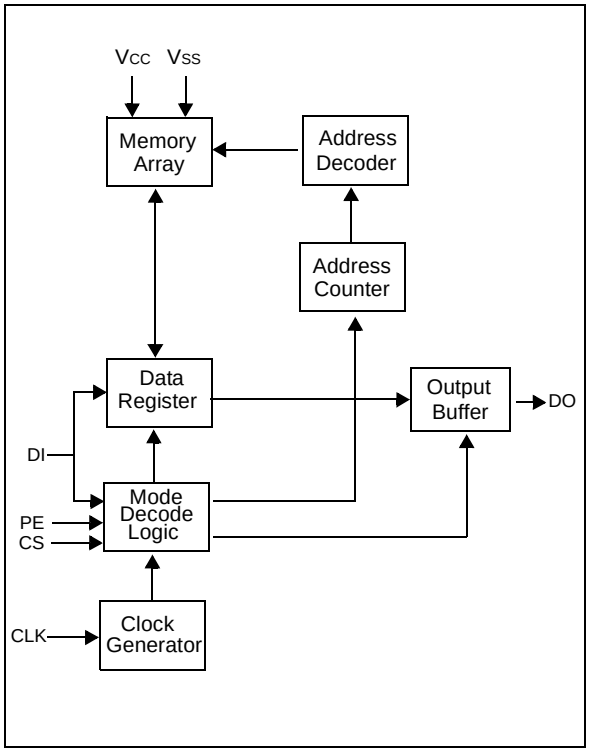
PDIP Package



SOIC Package



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

V_{CC}.....7.0V

All inputs and outputs w.r.t. V_{SS} .....-0.6V to Vcc + 1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

Soldering temperature of leads (10 seconds) .....+300°C

ESD protection on all pins.....4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

1.1 AC Test Conditions

AC Waveform:

V_{LO} = 2.0V

V_{HI} = Vcc - 0.2V **(Note 1)**

V_{HI} = 4.0V for **(Note 2)**

Timing Measurement Reference Level

Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For $V_{CC} \leq 4.0V$

2: For $V_{CC} > 4.0V$

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS	Applicable over recommended operating ranges shown below unless otherwise noted: V_{CC} = +2.5V to +6.0V Commercial (C): T_A = 0°C to +70°C Industrial (I): T_A = -40°C to +85°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
High-level input voltage	V_{IH1}	2.0	V_{CC} + 1	V	$V_{CC} \geq 2.7V$
	V_{IH2}	0.7 V_{CC}	V_{CC} + 1	V	$V_{CC} < 2.7V$
Low-level input voltage	V_{IL1}	-0.3	0.8	V	$V_{CC} \geq 2.7V$
	V_{IL2}	-0.3	0.2 V_{CC}	V	$V_{CC} < 2.7V$
Low-level output voltage	V_{OL1}	—	0.4	V	I_{OL} = 2.1 mA; V_{CC} = 4.5V
	V_{OL2}	—	0.2	V	I_{OL} =100 μA; V_{CC} = V_{CC} Min.
High-level output voltage	V_{OH1}	2.4	—	V	I_{OH} = -400 μA; V_{CC} = 4.5V
	V_{OH2}	V_{CC}-0.2	—	V	I_{OH} = -100 μA; V_{CC} = V_{CC} Min.
Input leakage current	I_{LI}	-10	10	μA	V_{IN} = 0.1V to V_{CC}
Output leakage current	I_{LO}	-10	10	μA	V_{OUT} = 0.1V to V_{CC}
Pin capacitance (all inputs/outputs)	C_{INT}	—	7	pF	**(Note 1)** T_A = +25°C, F_{CLK} = 1 MHz
Operating current	I_{CC} write	—	3	mA	V_{CC} = 5.5V
	I_{CC} read	—	1 500	mA μA	F_{CLK} = 3 MHz; V_{CC} = 5.5V F_{CLK} = 1 MHz; V_{CC} = 3.0V
Standby current	I_{CCS}	—	100 30	μA μA	CLK = CS = 0V; V_{CC} = 5.5V CLK = CS = 0V; V_{CC} = 3.0V DI = PE = V_{SS} ORG = V_{SS} or V_{CC}

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS	Applicable over recommended operating ranges shown below unless otherwise noted: V_{CC} = +2.5V to +6.0V Commercial (C): T_A = 0°C to +70°C Industrial (I): T_A = -40°C to +85°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Clock frequency	F_{CLK}	—	3 2	MHz MHz	4.5V ≤ V_{CC} ≤ 6.0V 2.5V ≤ V_{CC} < 4.5V
Clock high time	T_{CKH}	200 300	—	ns ns	4.5V ≤ V_{CC} ≤ 6.0V 2.5V ≤ V_{CC} < 4.5V
Clock low time	T_{CKL}	100 200	—	ns ns	4.5V ≥ V_{CC} ≤ 6.0V 2.5V ≤ V_{CC} < 4.5V
Chip select setup time	T_{CSS}	50 100	—	ns ns	4.5V ≤ V_{CC} ≤ 6.0V, Relative to CLK 2.5V ≤ V_{CC} < 4.5V, Relative to CLK
Chip select hold time	T_{CSH}	0	—	ns	—
Chip select low time	T_{CSL}	250	—	ns	Relative to CLK
Data input setup time	T_{DIS}	50 100	—	ns ns	4.5V ≤ V_{CC} ≤ 6.0V, Relative to CLK 2.5V ≤ V_{CC} <4.5V, Relative to CLK
Data input hold time	T_{DIH}	50 100	—	ns ns	4.5V ≤ V_{CC} ≤ 6.0V, Relative to CLK 2.5V ≤ V_{CC} < 4.5V, Relative to CLK
Data output delay time	T_{PD}	—	100 250	ns ns	4.5V ≤ V_{CC} ≤ 6.0V, C_L = 100 pF 2.5V ≤ V_{CC} < 4.5V, C_L = 100 pF
Data output disable time	T_{CZ}	—	100 500	ns ns	4.5V ≤ V_{CC} ≤ 6.0V 2.5V ≤ V_{CC} < 4.5V **(Note 1)**
Status valid time	Tsv	—	200 300	ns ns	4.5V ≥ V_{CC} ≤ 6.0V, C_L = 100 pF 2.5V ≤ V_{CC} <4.5V, C_L = 100 pF
Program cycle time	T_{WC}	—	5	ms	Erase/Write mode
	T_{EC}	—	15	ms	ERAL mode
	T_{WL}	—	30	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block mode **(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

TABLE 1-3: INSTRUCTION SET FOR 93LC76: ORG=1 (1X16 ORGANIZATION)

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
READ	1	10	X	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	29
EWEN	1	00	1	1	X	X	X	X	X	X	X	X	—	High-Z	13
ERASE	1	11	X	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	13
ERAL	1	00	1	0	X	X	X	X	X	X	X	X	—	(RDY/BSY)	13
WRITE	1	01	X	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0	1	X	X	X	X	X	X	X	X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0	0	X	X	X	X	X	X	X	X	—	High-Z	13

TABLE 1-4: INSTRUCTION SET FOR 93LC76: ORG=0 (X8 ORGANIZATION)

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
READ	1	10	X	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	22
EWEN	1	00	1	1	X	X	X	X	X	X	X	X		—	High-Z	14
ERASE	1	11	X	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	14
ERAL	1	00	1	0	X	X	X	X	X	X	X	X		—	(RDY/BSY)	14
WRITE	1	01	X	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0	1	X	X	X	X	X	X	X	X		D7 - D0	(RDY/BSY)	22
EWDS	1	00	0	0	X	X	X	X	X	X	X	X		—	High-Z	14

TABLE 1-5: INSTRUCTION SET FOR 93LC86: ORG=1 (X16 ORGANIZATION)

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
READ	1	10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	29
EWEN	1	00	1	1	X	X	X	X	X	X	X	X	—	High-Z	13
ERASE	1	11	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	13
ERAL	1	00	1	0	X	X	X	X	X	X	X	X	—	(RDY/BSY)	13
WRITE	1	01	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0	1	X	X	X	X	X	X	X	X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0	0	X	X	X	X	X	X	X	X	—	High-Z	13

TABLE 1-6: INSTRUCTION SET FOR 93LC86: ORG=0 (X8 ORGANIZATION)

Instruction	SB	Opcode	Address											Data In	Data Out	Req. CLK Cycles
READ	1	10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	22
EWEN	1	00	1	1	X	X	X	X	X	X	X	X		—	High-Z	14
ERASE	1	11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	14
ERAL	1	00	1	0	X	X	X	X	X	X	X	X		—	(RDY/BSY)	14
WRITE	1	01	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0	1	X	X	X	X	X	X	X	X		D7 - D0	(RDY/BSY)	22
EWDS	1	00	0	0	X	X	X	X	X	X	X	X		—	High-Z	14