DATA SHEET

TDA8580J
Multi-purpose power amplifier

Preliminary specification
Supersedes data of 1998 Feb 25
File under Integrated Circuits, IC01

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Philips
Semiconductors

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FEATURES

General

- Supply voltage range from 8 to 24 V
- Low distortion
- Few external components, fixed gain
- High output power
- Can be used as a stereo amplifier in Bridge-Tied Load (BTL) or quad Single-Ended (SE) amplifiers
- Single-ended mode without loudspeaker capacitor
- Mute and standby mode with one- or two-pin operation
- Diagnostic information for Dynamic Distortion Detector (DDD), high temperature (145 °C) and short-circuit
- No switch on/off plops when switching between standby and mute or mute and on; an external RC-network is prescribed to ensure plop-free operation
- Low offset variation at outputs between mute and on
- Fast mute on supply voltage drops.

Protection

- Short-circuit proof to ground, positive supply voltage and across load; the supply voltage ranges where the different short circuit conditions are guaranteed are given in Chapter “Limiting values”
- ESD protected on all pins
- Thermal protection against temperatures exceeding 150 °C.

GENERAL DESCRIPTION

The TDA8580J is a stereo Bridge-Tied Load (BTL) or a quad Single-Ended (SE) amplifier that operates over a wide supply voltage range from 8 to 24 V. This makes it suitable for applications such as television, home-sound systems and active speakers.

Because of an internal voltage buffer, this device can be used without a capacitor connected in series with the load (SE application). A combined BTL and 2 × SE application can also be configured (one chip stereo and subwoofer application).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8580J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		8.0	14.4	24	V
$I_{q(tot)}$	total quiescent current	V_P = 14.4 V	–	140	170	mA
I_{stb}	standby supply current	V_P = 14.4 V	–	1	50	µA
Bridge-tied load application						
G_v	voltage gain		31	32	33	dB
P_o	output power	THD = 0.5%; V_P = 14.4 V; R_L = 4 Ω	14	15	–	W
		THD = 0.5%; V_P = 24 V; R_L = 8 Ω	21	23	–	W
THD	total harmonic distortion	f_i = 1 kHz; P_o = 1 W; V_P = 14.4 V; R_L = 4 Ω	–	0.05	0.1	%
		f_i = 1 kHz; P_o = 10 W; V_P = 24 V; R_L = 8 Ω	–	0.02	0.05	%
$V_{offset(DC)}$	DC output offset voltage	V_P = 14.4 V; mute condition; R_L = 4 Ω	–	10	20	mV
		V_P = 14.4 V; on condition	–	0	140	mV
V_{no}	noise output voltage	R_S = 1 kΩ; V_P = 14.4 V	–	100	150	µV
SVRR	supply voltage ripple rejection	f_i = 1 kHz; $V_{ripple(p-p)}$ = 2 V; on or mute condition; R_S = 0 Ω	50	60	–	dB
Single-ended application						
G_v	voltage gain		25	26	27	dB
P_o	output power	THD = 0.5%; V_P = 14.4 V; R_L = 4 Ω	3.8	4.0	–	W
		THD = 0.5%; V_P = 24 V; R_L = 4 Ω	10.5	11.5	–	W
$V_{offset(DC)}$	DC output offset voltage	V_P = 14.4 V; mute condition; R_L = 4 Ω	–	10	20	mV
		V_P = 14.4 V; on condition	–	0	100	mV
V_{no}	noise output voltage	R_S = 1 kΩ; V_P = 14.4 V	–	80	120	µV
SVRR	supply voltage ripple rejection	f_i = 1 kHz; $V_{ripple(p-p)}$ = 2 V; on or mute condition; R_S = 0 Ω	40	45	–	dB

BLOCK DIAGRAM

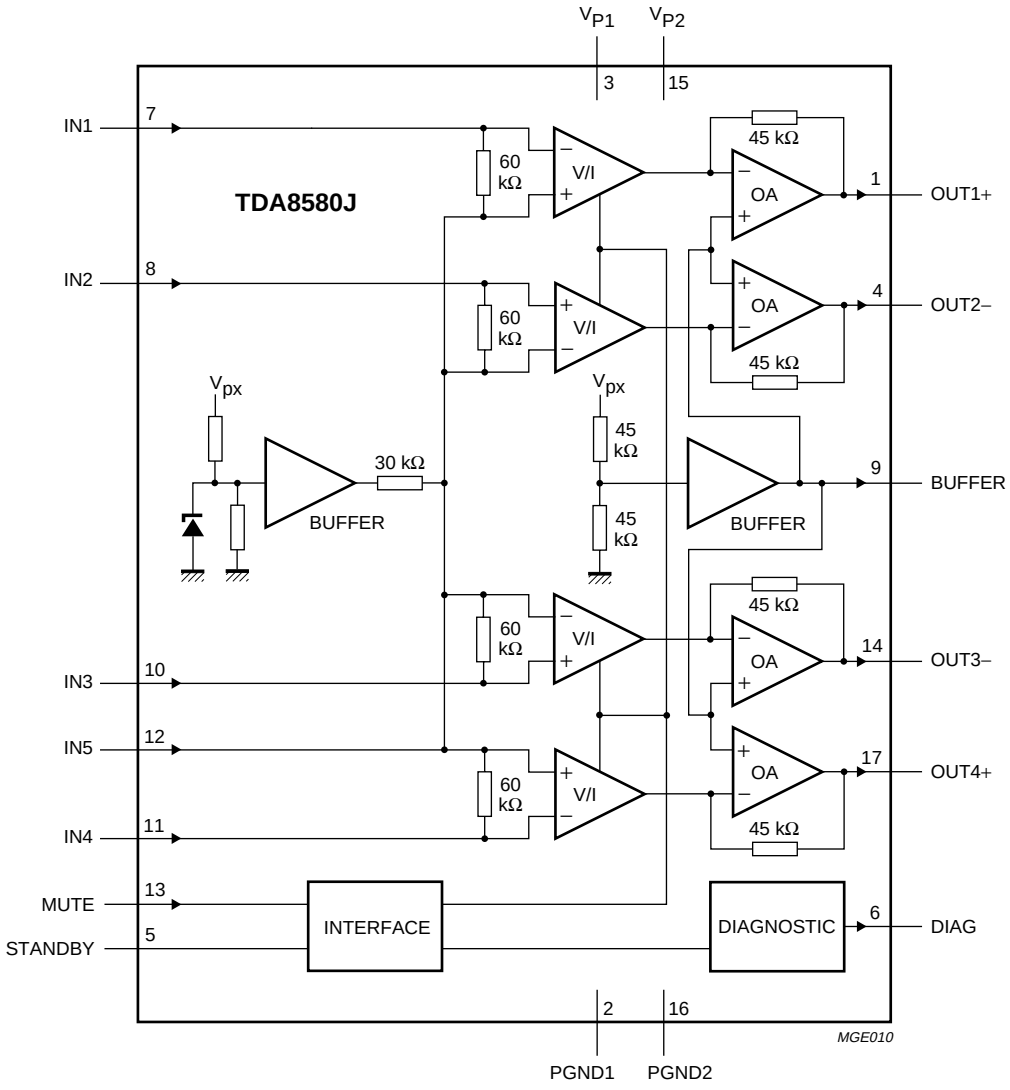

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT1+	1	non-inverting output 1
PGND1	2	power ground 1
V_{P1}	3	supply voltage 1
OUT2–	4	inverting output 2
STANDBY	5	standby/mute/on selection input
DIAG	6	diagnostic output
IN1	7	input 1
IN2	8	input 2
BUFFER	9	single-ended buffer output
IN3	10	input 3
IN4	11	input 4
IN5	12	input 5; signal ground capacitor connection
MUTE	13	mute/on selection input
OUT3–	14	inverting output 3
V_{P2}	15	supply voltage 2
PGND2	16	power ground 2
OUT4+	17	non-inverting output 4

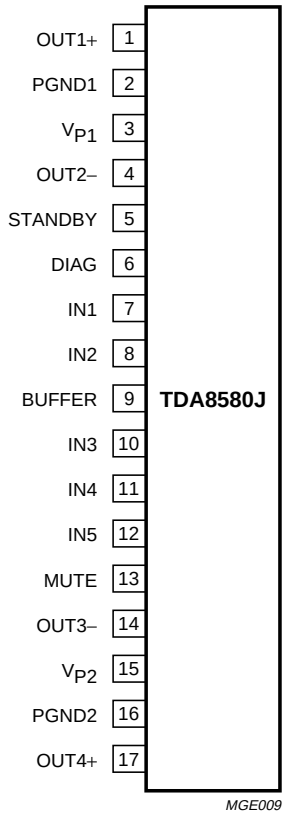

Fig.2 Pin configuration.