PS219A4-ASTX

Transfer-Mold Type
Insulated Type

Pre.	Zhang,T.Nagahara, T.Iwagami	Rev.	A	Zhang, T.Nagahara, T.Iwagami
Apr.	H.Yamamoto 21-Jun-'10	Apr.		H. Yamamoto 25-Oct-'10

Applications : AC100V~240V three phase low power motor inverter drive.

Integrated Power Functions :

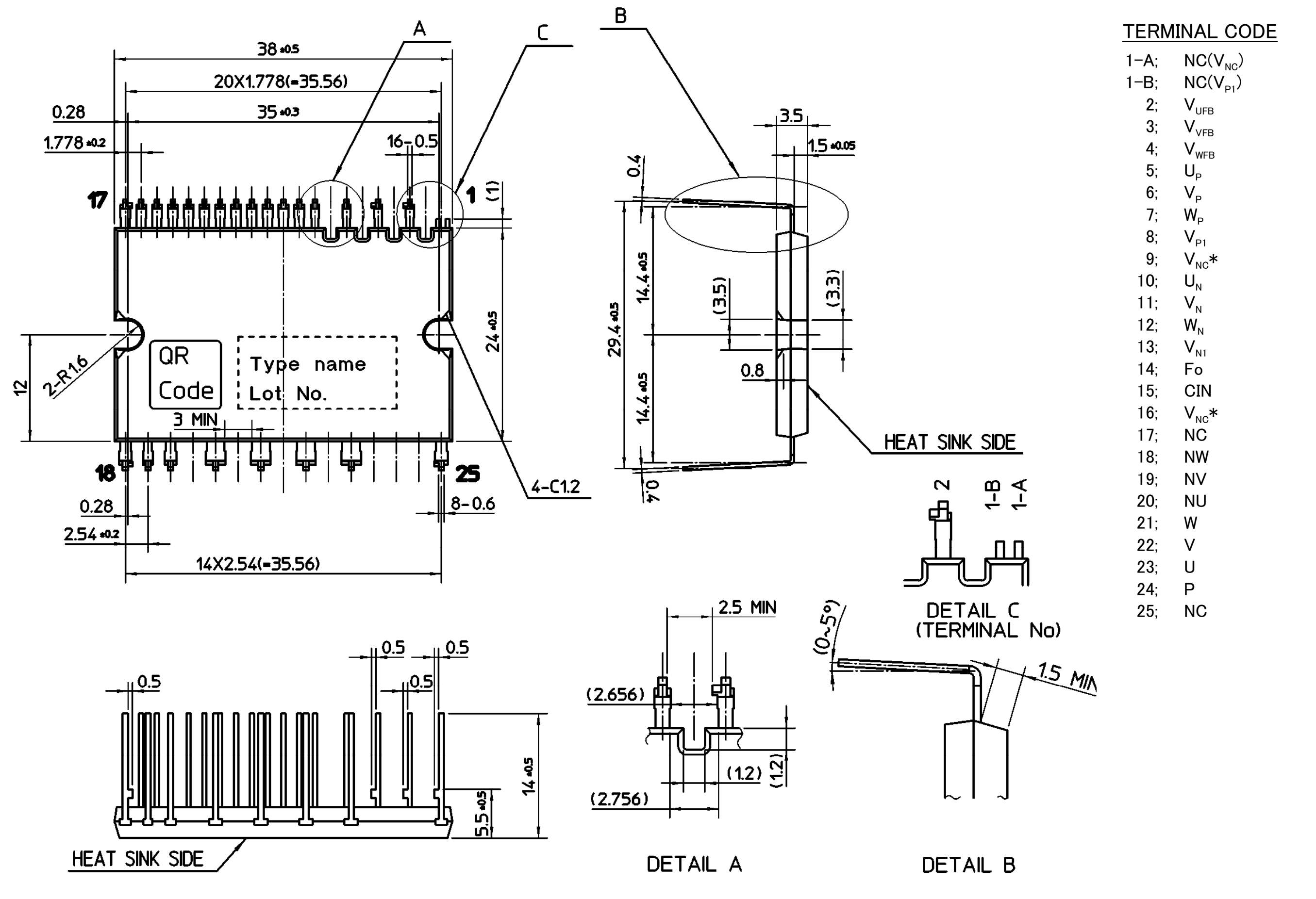
600V/15A low-loss IGBT inverter bridge for three phase DC-to-AC power conversion.
Built-in Bootstrap Di. Open Emitter type

Integrated drive, protection and system control functions :

-For P-side : Drive circuit, High voltage high-speed level shifting,
Control supply under-voltage (UV) protection.
-For N-side : Drive circuit, Control supply under-voltage protection (UV),
Short circuit protection (SC), Over temperature protection (OT).
-Fault signaling : Corresponding to a SC fault (N-side IGBT), a UV fault (N-side supply) or OT fault (LVIC temperature)
-Input interface : 3~5V line (High Active).

Fig. 1 Package Outlines PS219A4-ASTX

Dimensions in mm



*) Please use either one only of the two VNC pins (No.9, 16) for the ground connection and leave another one open.
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Maximum Ratings (Tj=25°C, unless otherwise noted)

Inverter Part

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	Applied between P-NU,NV,NW	450	V
Supply voltage (surge)	$V_{CC(surge)}$	Applied between P-NU,NV,NW	500	V
Collector-emitter voltage	V_{CES}		600	V
Each IGBT collector current	$\pm I_C$	Tc=25°C	15	A
Each IGBT collector current (peak)	$\pm I_{CP}$	Tc=25°C, less than 1ms	30	A
Collector dissipation A	P_C	Tc=25°C, per 1 chip	32.3	W
Junction temperature	Tj	(Note 1)	−20～+125	°C

(Note1)
The maximum junction temperature rating of the power chips integrated within the DIPIPM is 150°C(@Tc≤100°C). However, to ensure safe operation of the DIPIPM, the average junction temperature should be limited to Tj(ave)≤125°C (@Tc≤100°C).

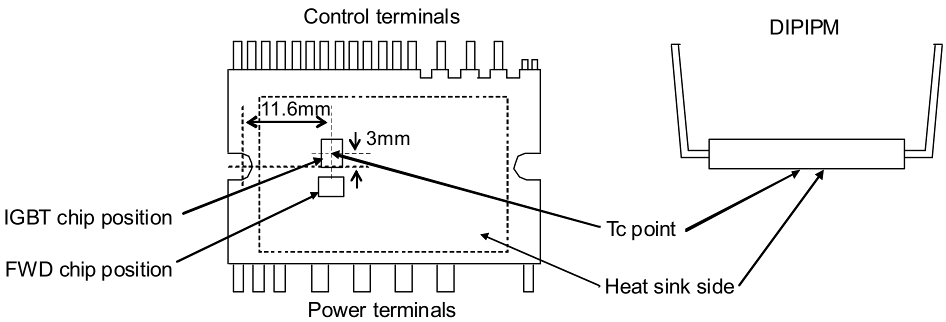
Control (Protection) Part

Item	Symbol	Condition	Rating	Unit
Control supply voltage	V_D	Applied between V_{P1}-V_{NC},V_{N1}-V_{NC}	20	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	20	V
Input voltage	V_{IN}	Applied between U_P,V_P,W_P-V_{NC}, U_N,V_N,W_N-V_{NC}	-0.5~V_D+0.5	V
Fault output supply voltage	V_{FO}	Applied between Fo-V_{NC}	-0.5~V_D+0.5	V
Fault output current	I_{FO}	Fo terminal sink current	1	mA
Current sensing input voltage	V_{SC}	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

Total System

Item	Symbol	Condition	Rating	Unit
Supply voltage self protection limit (short circuit protection capability)	$V_{CC(PROT)}$	V_D=13.5~16.5V, Inverter part Tj=125°C, non-repetitive less than 2μs	400	V
Module case operation temperature	Tc	(Note 2)	-20~+100	°C
Storage temperature	Tstg		-40~+125	°C
Isolation voltage	Viso	60Hz, Sinusoidal 1 minute, All connected pins to heat-sink plate	1500	Vrms

(Note 2) Tc measurement position A



Thermal Resistance

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case thermal A	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6 module)	-	-	3.1	°C/W
resistance A(Note 3)	$R_{th(j-c)F}$	Inverter FWD part (per 1/6 module)	-	-	4.5	

(Note 3) Grease with good thermal conductivity and long-term quality should be applied evenly with +100μm~+200μm on the contacting surface of DIPIPM and heat-sink. The contacting thermal resistance between DIPIPM case and heat sink ($R_{th(c-f)}$) is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ (per 1/6 module) is about 0.3°C/W when the grease thickness is 20μm and the thermal conductivity is 1.0W/m·k

Electrical Characteristics (Tj=25°C, unless otherwise noted.)

Inverter Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage [A]	$V_{CE(sat)}$	$V_D=V_{DB}$=15V	Tj=25°C	-	1.60	2.10	V
		I_C=15A, V_{IN}=5V	Tj=125°C	-	1.70	2.20	
FWD forward voltage [A]	V_{EC}	$-I_C$=15A, V_{IN}=0V		-	1.90	2.40	V
Switching times [A]	t_{on}	V_{CC}=300V, $V_D=V_{DB}$=15V		-	0.85	1.25	μs
	t_{rr}	I_C=15A, Tj=125°C		-	0.30	-	
	$t_{c(on)}$	V_{IN}=0-5V		-	0.40	0.60	
	t_{off}	Inductive load		-	1.10	1.50	
	$t_{c(off)}$			-	0.30	0.60	
Collector-emitter cut-off current	I_{CES}	$V_{CE}=V_{CES}$	Tj=25°C	-	-	1	mA
			Tj=125°C	-	-	10	

Control (Protection) Part

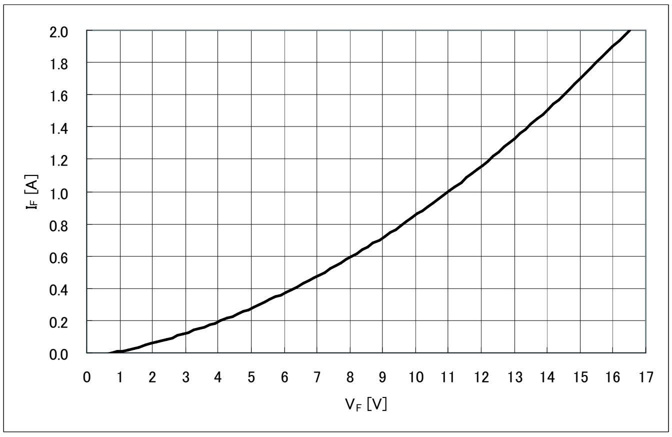
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit current	I_D	$V_D=V_{DB}$=15V V_{IN}=5V	Total of V_{P1}-V_{NC},V_{N1}-V_{NC}	-	-	2.80	mA
			V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	-	-	0.10	
		$V_D=V_{DB}$=15V V_{IN}=0V	Total of V_{P1}-V_{NC},V_{N1}-V_{NC}	-	-	2.80	
			V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	-	-	0.10	
Fault output voltage	V_{FOH}	V_{SC}=0V,Fo terminal pull-up to 5V by 10kΩ		4.9	-	-	V
	V_{FOL}	V_{SC}=1V, I_{FO}=1mA		-	-	0.95	
Input current	I_{IN}	V_{IN}=5V		0.70	1.00	1.50	mA
Over temperature Protection (Note6)	OT_t	V_D=15V,	Trip level	100	120	140	℃
	OT_{rh}	At temperature of LVIC	Trip/reset hysteresis	-	10	-	
Short circuit trip level	$V_{SC(ref)}$	V_D=15V	(Note 4)	0.43	0.48	0.53	V
Control supply under-voltage protection	UV_{DBt}	Tj≤125°C	Trip level	7.0	10.0	12.0	V
	UV_{DBr}		Reset level	7.0	10.0	12.0	
	UV_{Dt}		Trip level	10.3	-	12.5	
	UV_{Dr}		Reset level	10.8	-	13.0	
Fault output pulse width	t_{FO}		(Note 5)	20	-	-	μs
ON threshold voltage	$V_{th(on)}$	Applied between U_P,V_P,W_P,U_N,V_N,W_N-V_{NC}		-	2.1	2.6	V
OFF threshold voltage	$V_{th(off)}$			0.8	1.3	-	
ON/OFF threshold hysteresis voltage	$V_{th(hys)}$			0.35	0.65	-	
Boot strap Di forward voltage (Note 7)	V_F	IF=100mA		2.1	2.8	3.5	V

(Note 4) Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

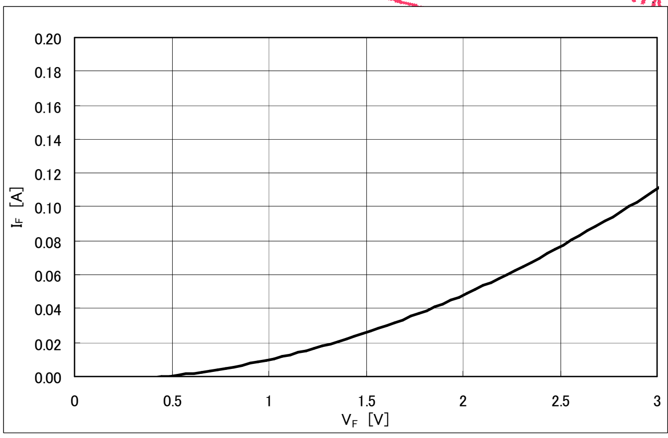
(Note 5) Fault signal is asserted only corresponding to a SC or a UV failure at lower side, and the Fo pulse width is different for each failure modes. For SC failure, Fo output is with a fixed width of 20μs(min), but for UV failure, Fo output continuously during the whole UV period, however, the minimum Fo pulse width is 20μs(min) for very short UV period less than 20μs.

(Note 6) Over temperature protection(OT) outputs fault signal, when the LVIC temperature exceeds OT trip temperature level(OT_t). In that case if the heat sink comes off DIPIPM or fixed loosely, don't reuse that DIPIPM. (There is a possibility that junction temperature of power chips exceeded maximum Tj(150°C).

(Note 7) It is recommended for the bootstrap capacitance to be 22μF or below. If it exceeds 22μF by the control condition, please refer the application note for this product (document No.DPH-7111e) that describes about the usage of built-in bootstrap diode or contact us. The characteristic of bootstrap Di is described below.



V_F–I_F curve for bootstrap

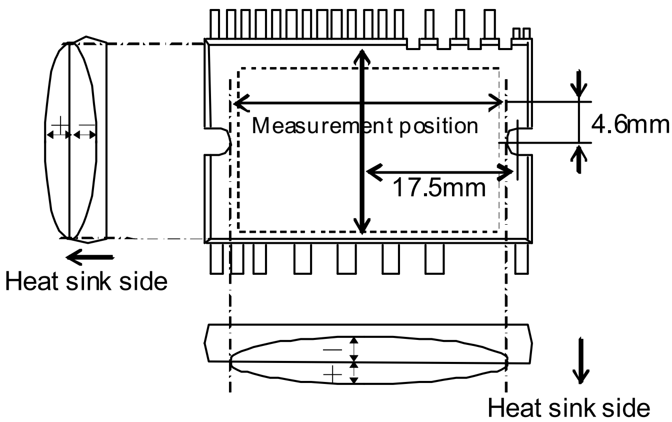


Di V_F–I_F curve for bootstrap Di (magnified view)

Mechanical Characteristics and Ratings

Item	Condition			Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: M3 (Note 8)	Recommended: 0.69N·m	-	0.59	-	0.78	N·m
Terminal pulling strength	Control terminal: Weight 4.9N Power terminal: Weight 9.8N		EIAJ-ED-4701	-	10	-	s
Terminal bending strength	Control terminal: Weight 2.45N Power terminal: Weight 4.9N 90deg. bend		EIAJ-ED-4701	-	2	-	times
Weight			-	-	10	-	g
Heat-sink flatness	(Note 9)		-	-50	-	+100	μm

(Note 8) Plain washers (ISO 7089~7094) are recommended.
(Note 9) Flatness measurement position: A



Recommended Operation Conditions

Item	Symbol	Condition		Recommended Min.	Recommended Typ.	Recommended Max.	Unit
Supply voltage	V_{CC}	Applied between P-NU,NV,NW		0	300	400	V
Control supply voltage	V_D	Applied between V_{P1}-V_{NC},V_{N1}-V_{NC}		13.5	15.0	16.5	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		13.0	15.0	18.5	V
Control supply variation	ΔV_D,ΔV_{DB}			-1	-	1	V/μs
Arm-shoot-through blocking time	t_{dead}	For each input signal, Tc≤100°C		1.0	-	-	μs
Allowable r.m.s. current A	I_O	V_{CC}=300V, V_D=V_{DB}=15V, P.F=0.8, sinusoidal PWM, Tj≤125°C, Tc≤100°C (Note10)	f_{PWM}=5kHz	-	-	7.5	Arms
			f_{PWM}=15kHz	-	-	4.5	
Allowable minimum input pulse width	PWIN(on)	(Note 11)		0.5	-	-	μs
	PWIN(off)			0.5	-	-	
V_{NC} variation	V_{NC}	Between V_{NC}- NU,NV,NW (including surge)		-5.0	-	5.0	V
Junction temperature	Tj			-20	-	125	°C

(Note 10) The allowable r.m.s. current also depends on the actual application conditons.

(Note 11) DIPIPM might not make response or work properly if the input signal pulse width is less than PWIN(on), PWIN(off). And if such a short ON signal pulse is input, it might cause excessive negative surge between output (U,V,W) and GND (VNC), or fluctuation of control supply voltage 15V. It is recommend that the total parastic inductance of shunt resistor and wiring between N terminal (N-side IGBT emitter) - GND(VNC) is 10nH or less and the ceramic capacitors with good temperature, frequency and DC bias characteristics are located nearby the control supply terminals (between VN1,VP1 and VNC).

Fig.2 DIPIPM Internal Circuit:

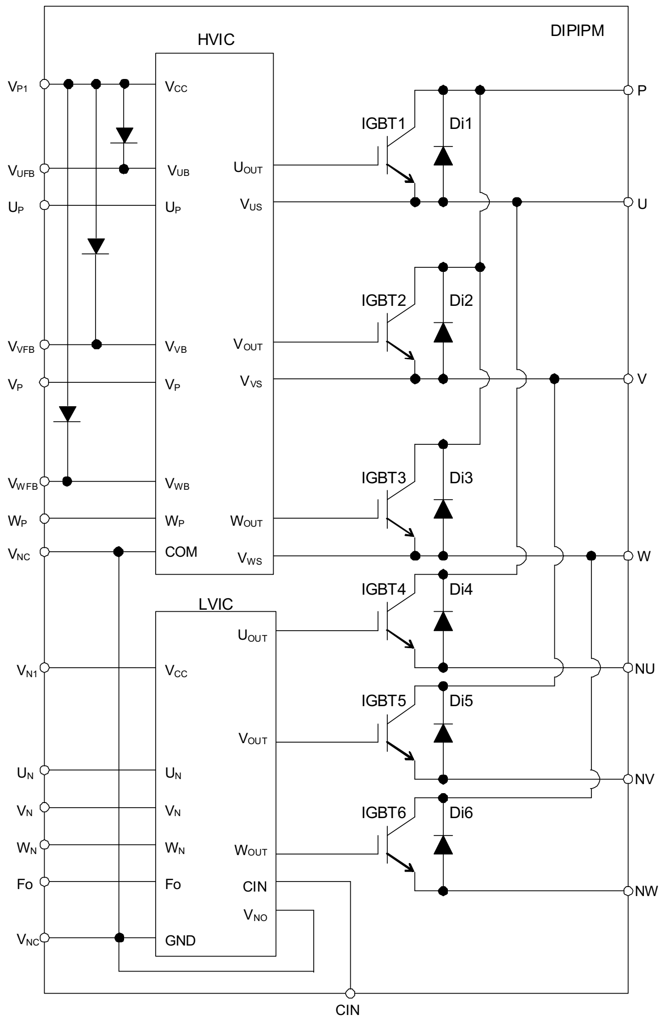
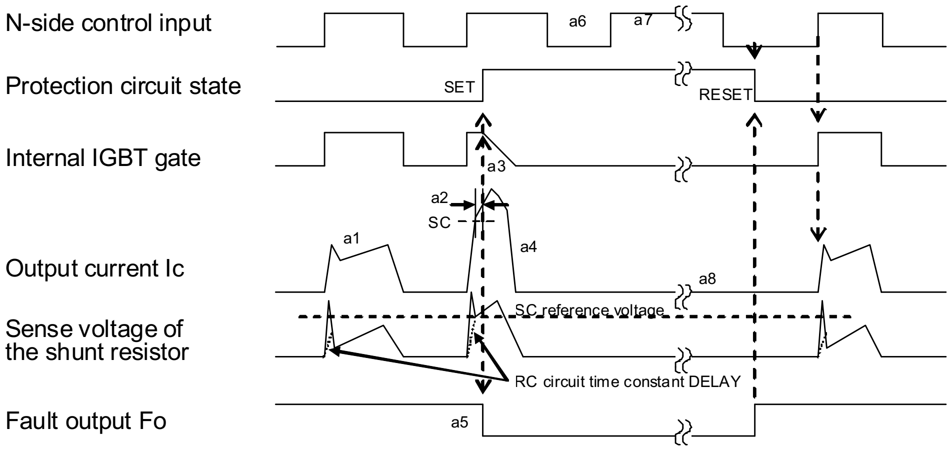


Fig.3 Timing Chart of the DIPIPM Protective Functions

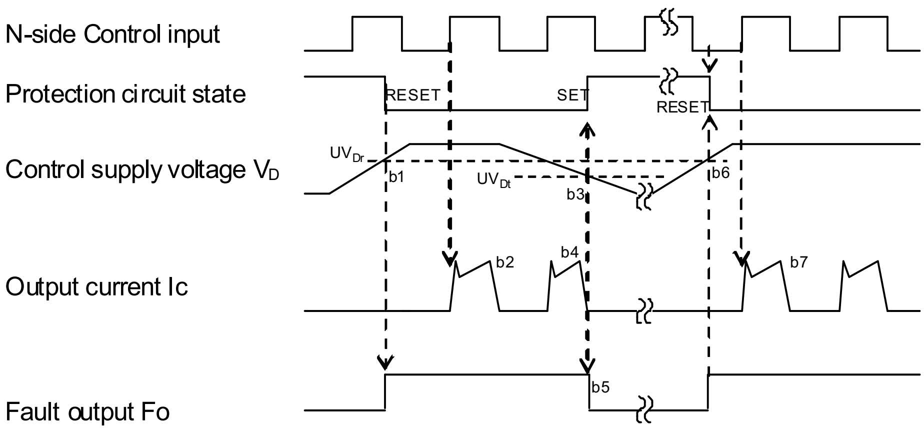
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: IGBT ON and carrying current.
a2. Short circuit detection (SC trigger).
a3. All N-side IGBT gate hard interruption.
a4. All N-side IGBTs turn OFF.
a5. Fo outputs with a fixed pulse width of ($t_{FO(min)}$=20μs).
a6. Input = “L”. IGBT OFF.
a7. Input = “H”.
a8. IGBT OFF in spite of “H” input.



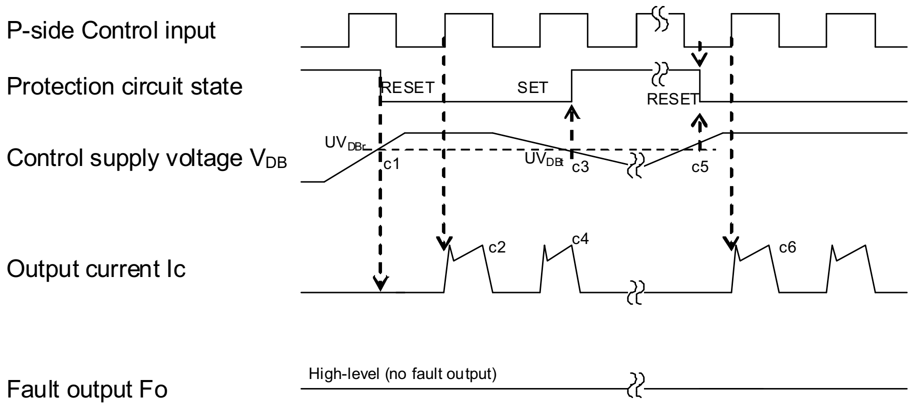
[B] Under Voltage Protection (N-side, UV_D)

b1. Control supply voltage rising: After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
b2. Normal operation : IGBT ON and carrying current.
b3. Under voltage trip (UV_{Dt}).
b4. All N-side IGBTs OFF in spite of control input condition.
b5. Fo outputs($t_{FO} \geq$ 20μs and Fo outputs continuously during under voltage UV period., however, the minimum pulse width is 20μs.)
b6. Under voltage reset (UV_{Dr}).
b7. Normal operation : IGBT ON and carrying current.



[C] Under Voltage Protection (P-side, UV_{DB})

c1. Control supply voltage rises: After the voltage reaches UV_{DBr}, the circuits start to operate when next input is applied.
c2. Normal operation : IGBT ON and carrying current.
c3. Under voltage trip (UV_{DBt}).
c4. P-side IGBT turns OFF in spite of control input signal level, but there is no Fo signal outputs.
c5. Under voltage reset (UV_{DBr}).
c6. Normal operation : IGBT ON and carrying current.



[D] Over Temperature Protection (N-side, OT)

d1. Normal operation: IGBT ON and carrying current
d2. LVIC temperature exceeds over temperature trip level(OT_t).
d3. All N-side IGBTs turn OFF in spite of control input condition.
d4. Fo outputs during over temperature period, however, the minimum pulse width is 20μs.
d5. LVIC temperature becomes under over temperature reset level.
d6. Circuits start to operate normally when next input is applied.

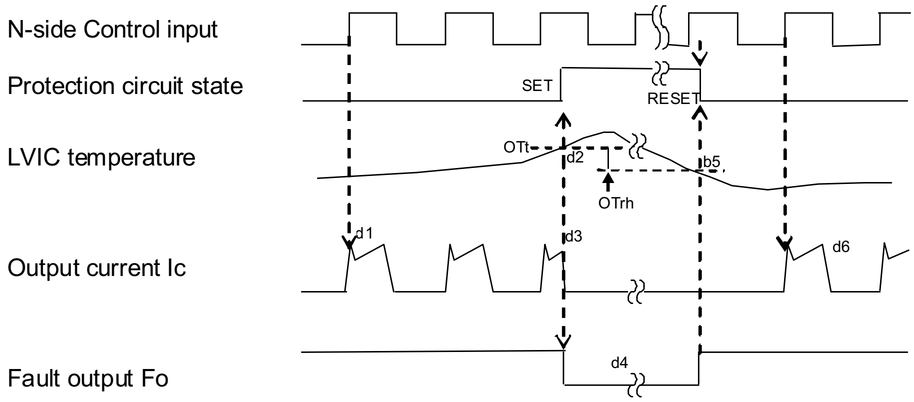
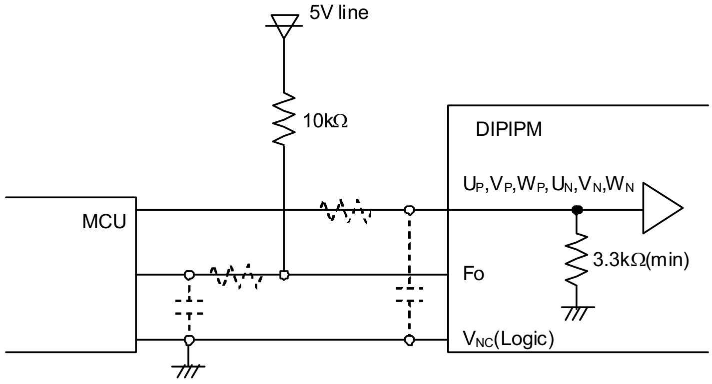


Fig.4 A Instance of Interface Circuit



Note:
1. The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.
2. The DIPIPM input section integrates a 3.3kΩ(min)pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

Fig.5 Pattern Wiring Around the Shunt Resistor

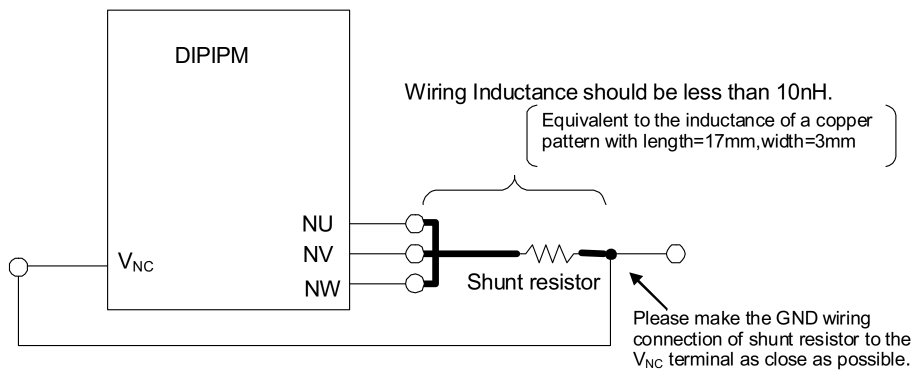
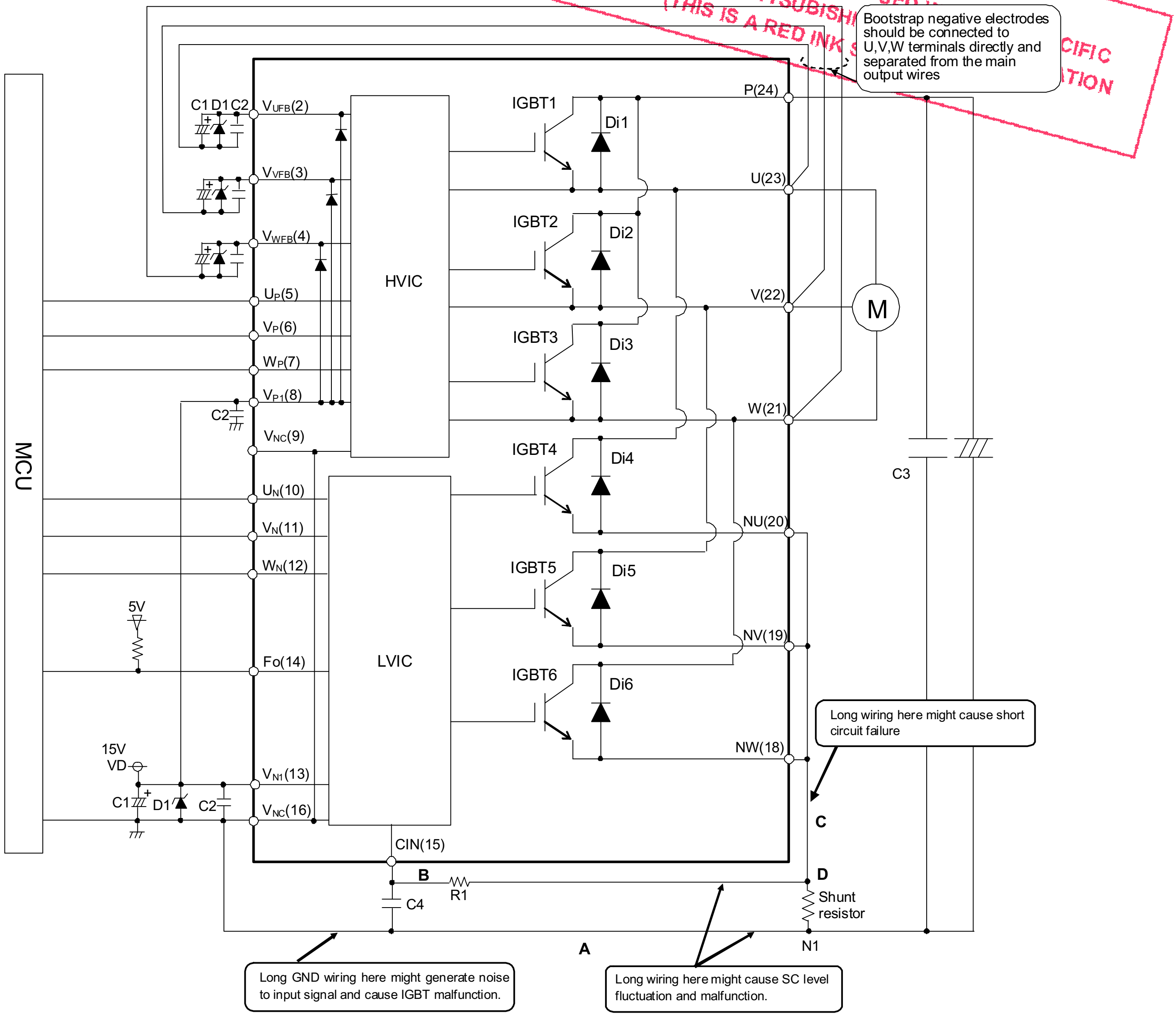


Fig.6 System Connection Example of DIPIPM Application Circuit (1 shunt resistor)



Note:

(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).

(2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.

(3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

(4) The time constant R1C4 of the protection circuit should be selected in the range of 1.5-2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1, C4.

(5) To prevent malfunction, the wiring of A, B, C should be as short as possible.

(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU,NV,NW terminals should be connected at near NU,NV,NW terminals.

(7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)

(8) Input drive is High-active type. There is a 3.3kΩ(Min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

(9) Fo output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V) by resistor makes I_{Fo} up to 1mA.

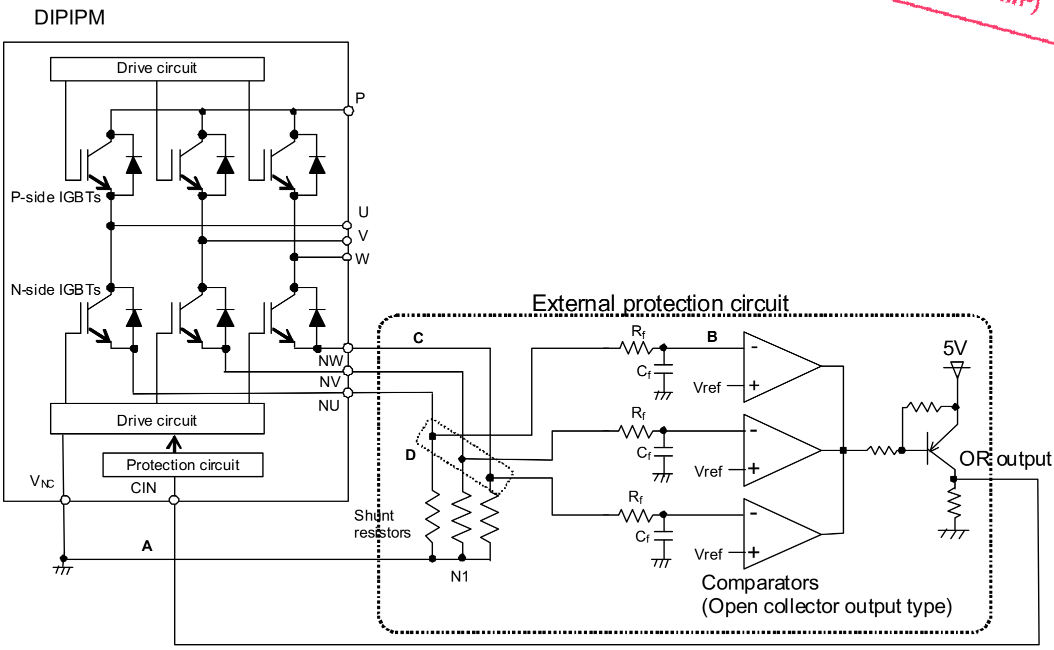
(10) Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

(11) Two VNC terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.

(12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.

(13) Please refer to application note (DPH-7111e) for the usage of BSD.

Fig.7 External SC Protection Circuit with Using Three Shunt Resistors



Note:

(1) It is necessary to set the time constant RfCf of external comparator input so that IGBT stop within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(2) The threshold voltage Vref should be set up the same rating of short circuit trip level (Vsc(ref) typ. 0.48V).
(3) Select the external shunt resistance so that SC trip-level is less than specified value.
(4) To avoid malfunction, the wiring A, B, C should be as short as possible.
(5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
(6) OR output high level should be over 0.53V (=maximum Vsc(ref)).

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