

HD74LS74A • Dual D-type Positive Edge-triggered Flip-Flops (with Preset and Clear)

FUNCTION TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\bar{Q}_0

Notes) H; high level, L; low level, X; irrelevant

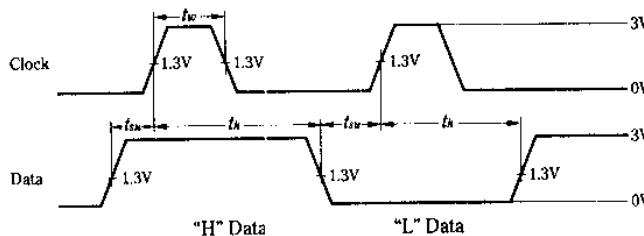
↑; transition from low to high level

Q_0 ; level of Q before the indicated steady-state conditions were established.

\bar{Q}_0 ; complement of Q_0 , or level of \bar{Q} before the indicated steady-state input conditions were established.

*; This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

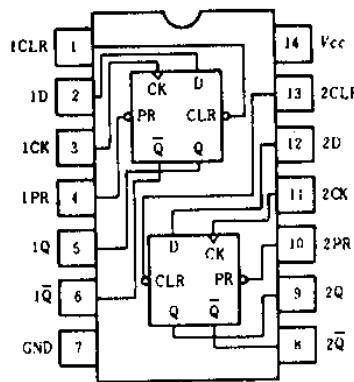
TIMING DEFINITION



ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ C$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}	$V_{CC} = 4.75V, V_{IL} = 2V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -400\mu A$	2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OL} = 8mA$	2.7	—	—	V
	V_{OL}		—	—	0.5	V
Input current	D	I_{IH}	—	—	20	
	Clear		—	—	40	μA
	Preset		—	—	40	
	Clock		—	—	20	
	D	I_{IL}	—	—	-0.4	
	Clear		—	—	-0.8	mA
	Preset		—	—	-0.8	
	Clock		—	—	-0.4	
	D	I_I	—	—	0.1	
	Clear		—	—	0.2	mA
	Preset		—	—	0.2	
	Clock		—	—	0.1	
Short-circuit output current	I_{OS}	$V_{CC} = 5.25V$	-20	—	-100	mA
Supply current	I_{CC}^{**}	$V_{CC} = 5.25V$	—	4	8	mA
Input clamp voltage	V_{IK}	$V_{CC} = 4.75V, I_{IN} = -18mA$	—	—	-1.5	V

PIN ARRANGEMENT



(Top View)

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	25	MHz
Pulse width	Clock High	t_W	25	—	—
	Clear/Preset		25	—	—
Setup time	"H" Data	t_{SU}	20↑	—	—
	"L" Data		20↑	—	—
Hold time	t_h	5↑	—	—	ns

Note) ↑; The arrow indicates the rising edge.

* $V_{CC}=5V, T_a=25^\circ C$

** With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.