P- Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME45P04-G is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 18m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 25m\Omega @ V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

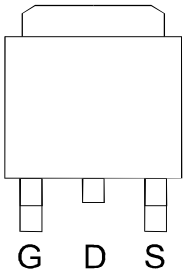
APPLICATIONS

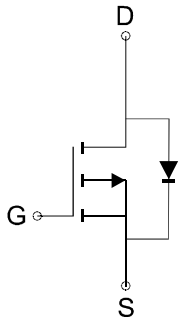
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-252)

Top View





P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Rating		Unit
Drain-Source Voltage		V_{DSS}	-40		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current(Tj=150℃)*	Tc=25℃	I_D	-30		A
	Tc=70℃		-23		
Pulsed Drain Current		I_{DM}	-100		A
Maximum Power Dissipation*	Tc=25℃	P_D	25		W
	Tc=70℃		16		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	Typ	40	℃/W
			Max	50	
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	5		℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper