2N3906

General Purpose Transistors

PNP Silicon

Features

- Pb−Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	40	Vdc
Collector − Base Voltage	V_{CBO}	40	Vdc
Emitter − Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_A = 60°C	P_D	250	mW
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS (Note 1)

| Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
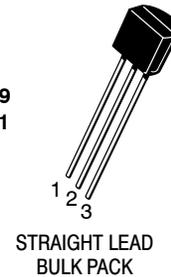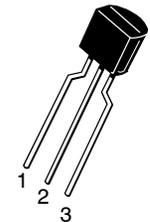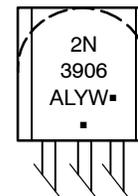1. Indicates Data in addition to JEDEC Requirements.

ON Semiconductor®

COLLECTOR
3

2
BASE

1
EMITTER
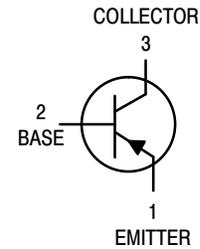
TO−92
CASE 29
STYLE 1

1
2
3
STRAIGHT LEAD
BULK PACK

1
2
3
BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAM

2N
3906
ALYW∎

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
∎ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (Note 2)	(I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	–	Vdc
Collector – Base Breakdown Voltage	(I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	40	–	Vdc
Emitter – Base Breakdown Voltage	(I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	–	Vdc
Base Cutoff Current	(V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{BL}	–	50	nAdc
Collector Cutoff Current	(V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{CEX}	–	50	nAdc
ON CHARACTERISTICS (Note 2)					
DC Current Gain	(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	60	–	–
	(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)		80	–	
	(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		100	300	
	(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		60	–	
	(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)		30	–	
Collector – Emitter Saturation Voltage	(I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	–	0.25	Vdc
	(I_C = 50 mAdc, I_B = 5.0 mAdc		–	0.4	
Base – Emitter Saturation Voltage	(I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	0.65	0.85	Vdc
	(I_C = 50 mAdc, I_B = 5.0 mAdc)		–	0.95	
SMALL – SIGNAL CHARACTERISTICS					
Current – Gain – Bandwidth Product	(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	250	–	MHz
Output Capacitance	(V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	–	4.5	pF
Input Capacitance	(V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ibo}	–	10	pF
Input Impedance	(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{ie}	2.0	12	kΩ
Voltage Feedback Ratio	(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{re}	0.1	10	X 10^{-4}
Small – Signal Current Gain	(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	100	400	–
Output Admittance	(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{oe}	3.0	60	μmhos
Noise Figure	(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	–	4.0	dB
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc, I_C = 10 mAdc, I_{B1} = 1.0 mAdc)	t_d	–	35	ns
Rise Time		t_r	–	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1.0 mAdc)	t_s	–	225	ns
Fall Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1.0 mAdc)	t_f	–	75	ns

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

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Device	Package	Shipping[†]
2N3906	TO−92	5000 Units / Bulk
2N3906G	TO−92 (Pb−Free)	5000 Units / Bulk
2N3906RL1	TO−92	2000 / Tape & Reel
2N3906RL1G	TO−92 (Pb−Free)	2000 / Tape & Reel
2N3906RLRA	TO−92	2000 / Tape & Reel
2N3906RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
2N3906RLRM	TO−92	2000 / Tape & Ammo Box
2N3906RLRMG	TO−92 (Pb−Free)	2000 / Tape & Ammo Box
2N3906RLRP	TO−92	2000 / Tape & Ammo Box
2N3906RLRPG	TO−92 (Pb−Free)	2000 / Tape & Ammo Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
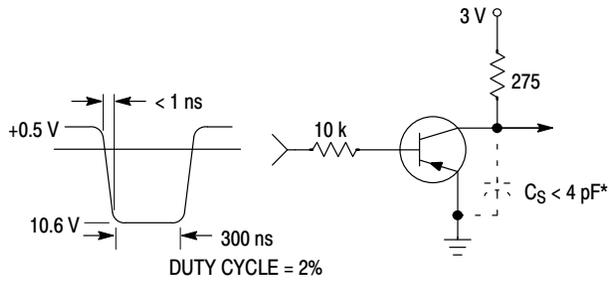
* Total shunt capacitance of test jig and connectors

Figure 1. Delay and Rise Time Equivalent Test Circuit
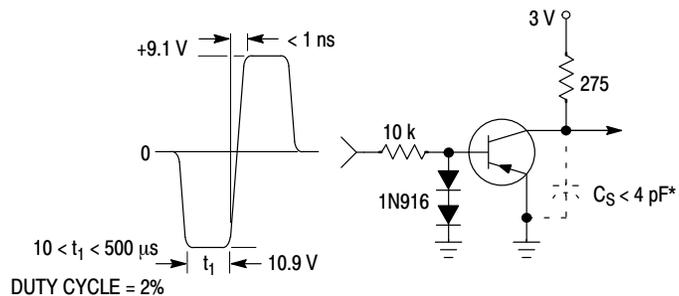
* Total shunt capacitance of test jig and connectors

Figure 2. Storage and Fall Time Equivalent Test Circuit

TYPICAL TRANSIENT CHARACTERISTICS

——— $T_J = 25°C$
— — — $T_J = 125°C$
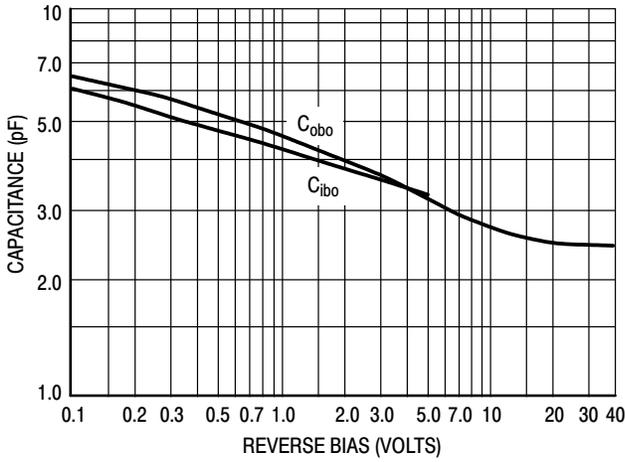
Figure 3. Capacitance
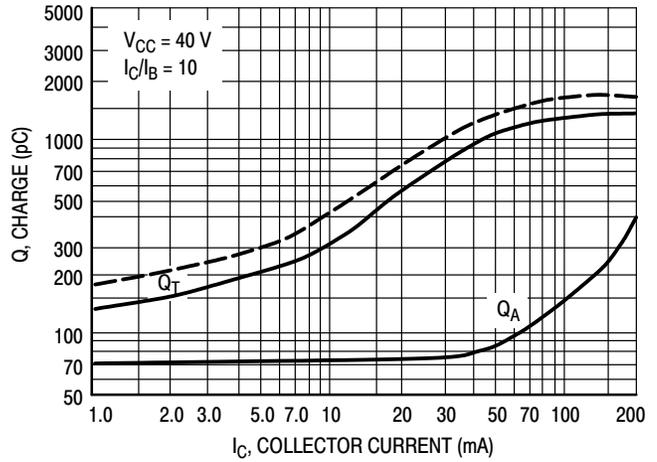
Figure 4. Charge Data
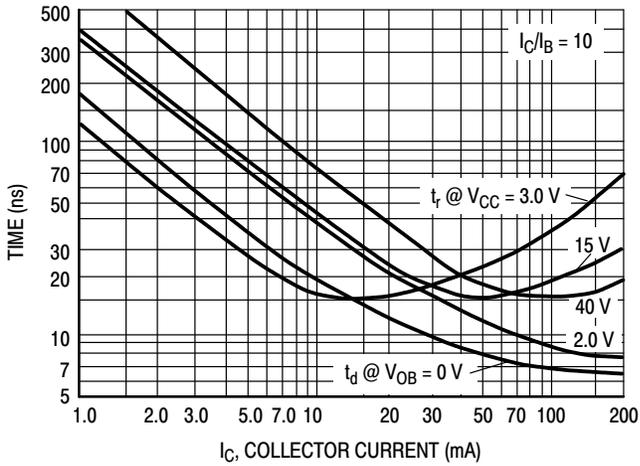
Figure 5. Turn–On Time
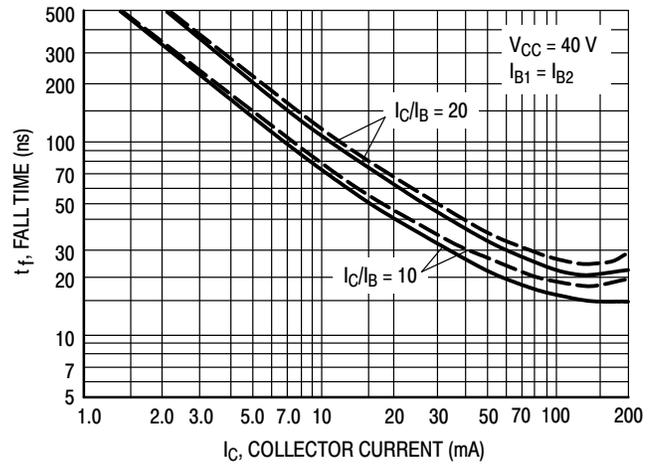
Figure 6. Fall Time

TYPICAL AUDIO SMALL–SIGNAL CHARACTERISTICS
NOISE FIGURE VARIATIONS
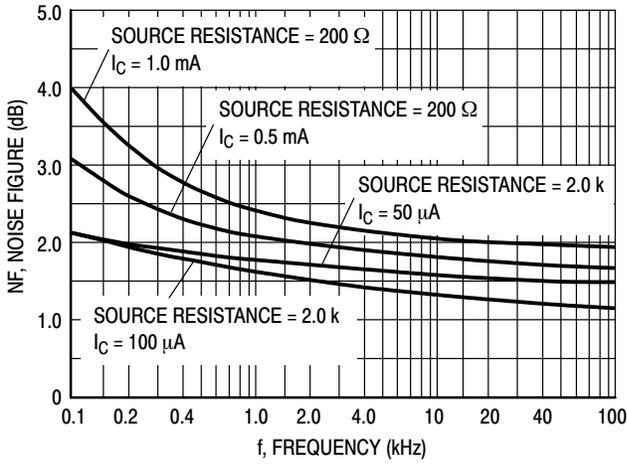
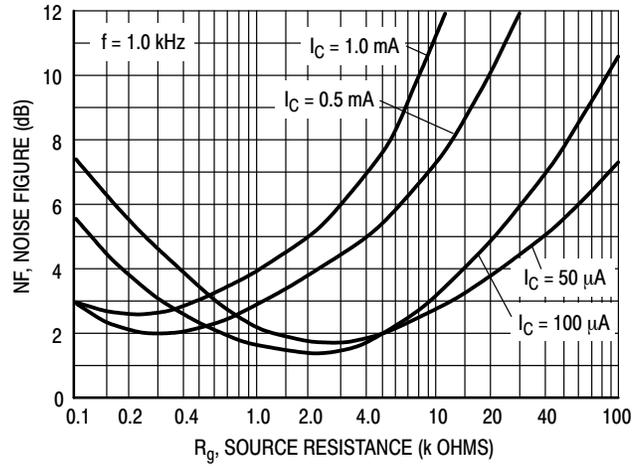(V_{CE} = − 5.0 Vdc, T_A = 25°C, Bandwidth = 1.0 Hz)

Figure 7.

Figure 8.

h PARAMETERS

(V_{CE} = − 10 Vdc, f = 1.0 kHz, T_A = 25°C)
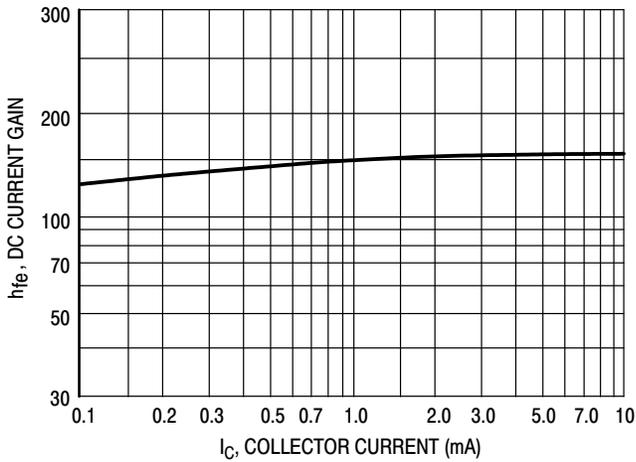
Figure 9. Current Gain
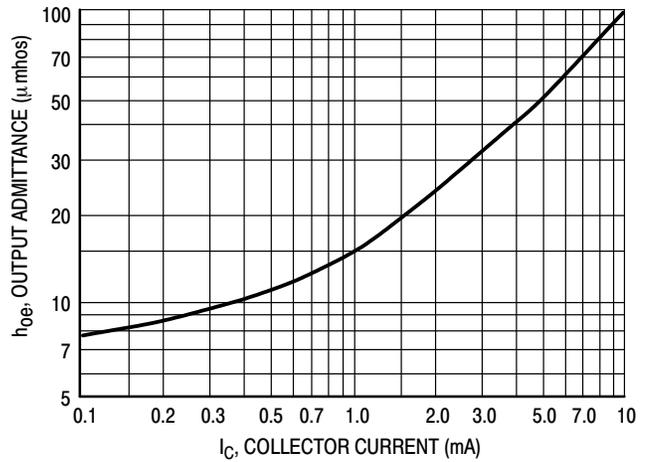
Figure 10. Output Admittance
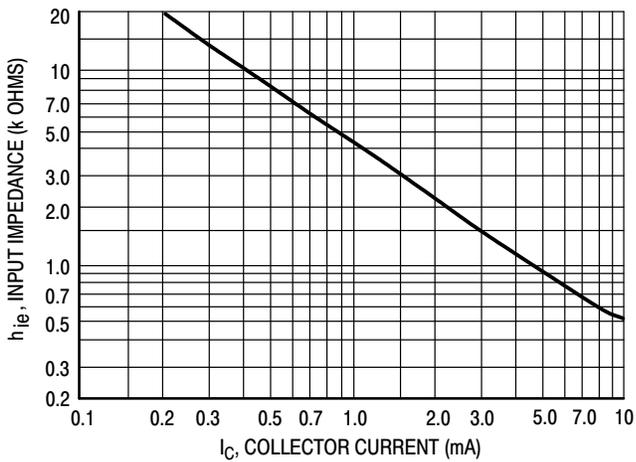
Figure 11. Input Impedance
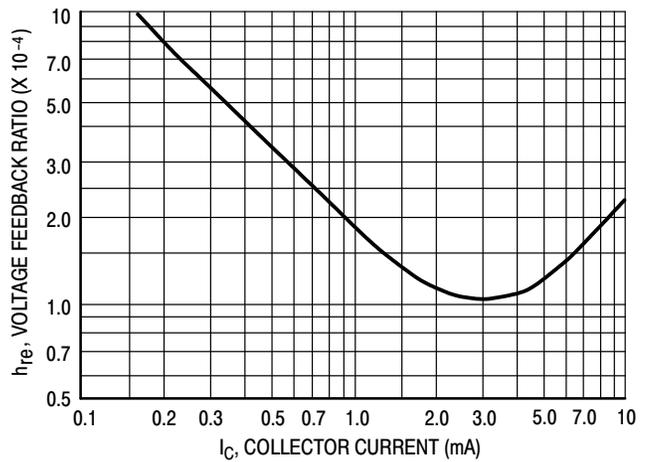
Figure 12. Voltage Feedback Ratio

2N3906

TYPICAL STATIC CHARACTERISTICS
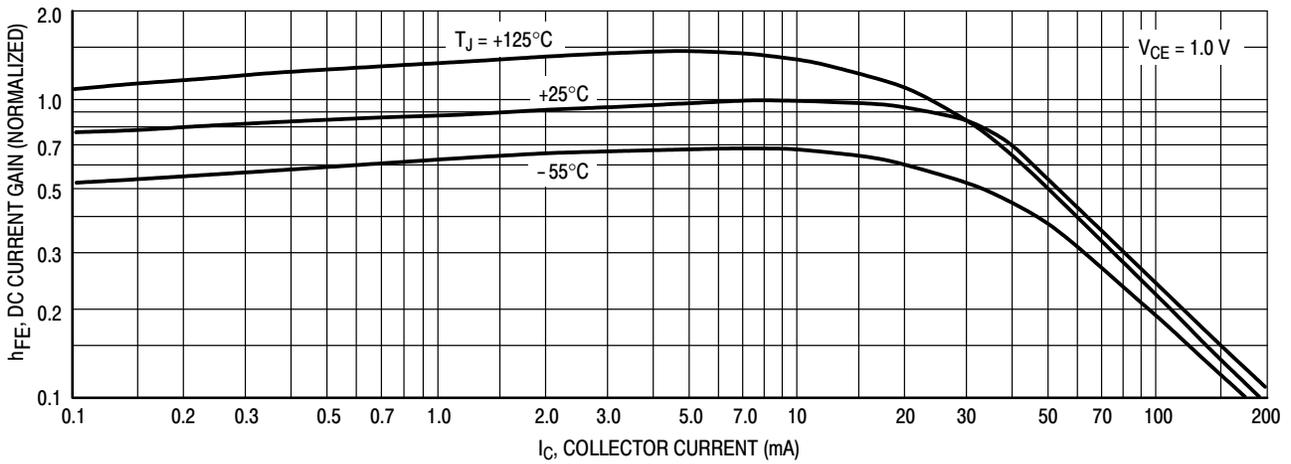
Figure 13. DC Current Gain
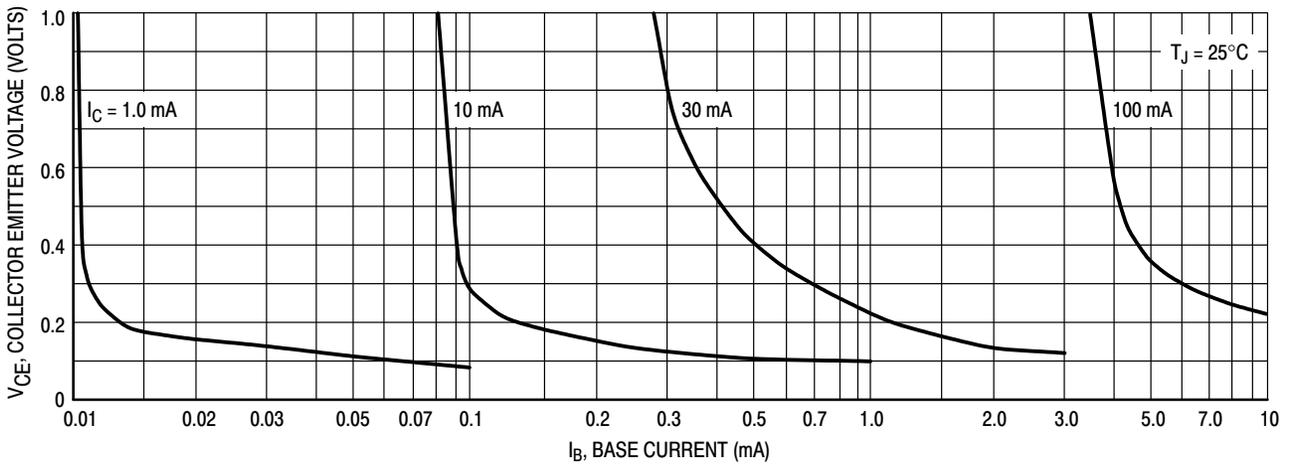
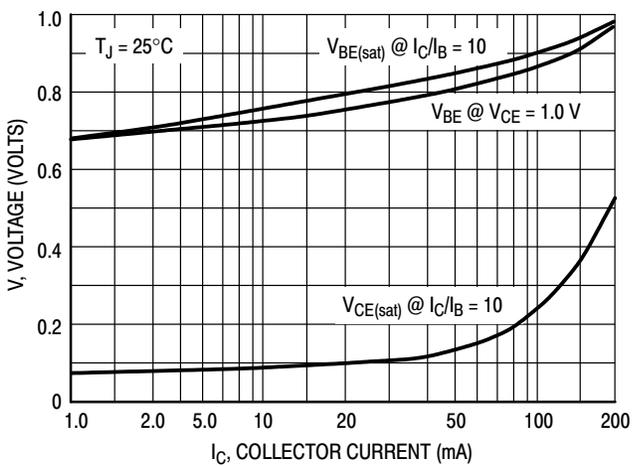

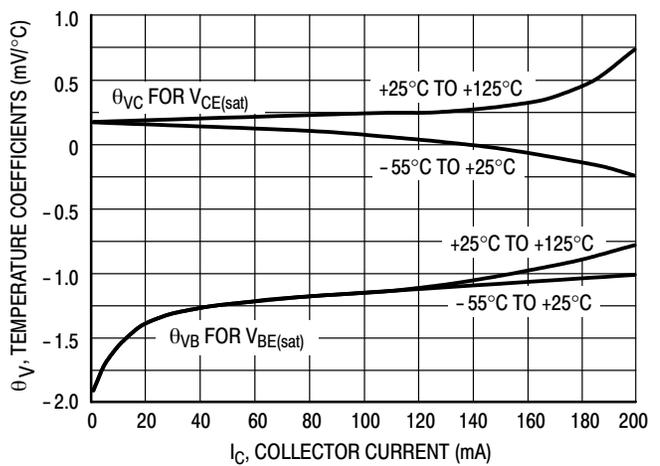**Figure 14. Collector Saturation Region**

Figure 15. "ON" Voltages

Figure 16. Temperature Coefficients

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK
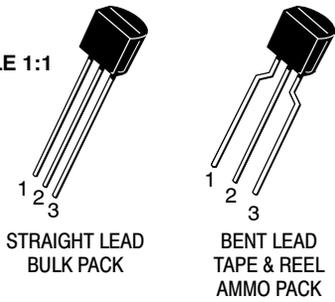
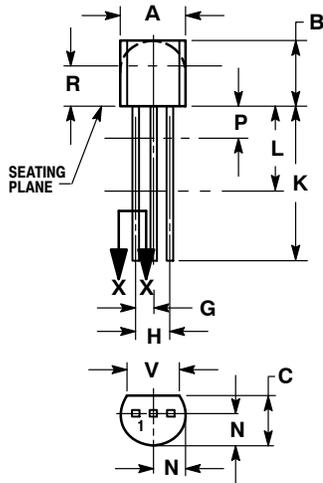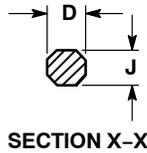**TO–92 (TO–226)**
CASE 29–11
ISSUE AM

DATE 09 MAR 2007
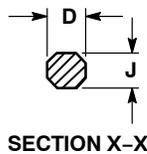

STRAIGHT LEAD
BULK PACK

SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

BENT LEAD
TAPE & REEL
AMMO PACK

SECTION X–X
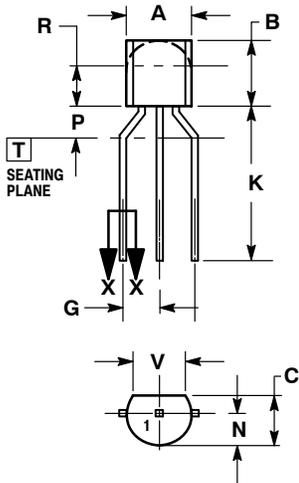
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42022B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO–92 (TO–226)	PAGE 1 OF 3

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

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STATUS:	**ON SEMICONDUCTOR STANDARD**	
NEW STANDARD:		
DESCRIPTION:	**TO–92 (TO–226)**	**PAGE 2 OF 3**

ISSUE	REVISION	DATE
AM	ADDED BENT−LEAD TAPE & REEL VERSION. REQ. BY J. SUPINA.	09 MAR 2007

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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