1. GENERAL DESCRIPTION

EM78P153S is an 8-bit microprocessor with low-power and high-speed CMOS technology. It is equipped with a 1024*13-bits Electrical One Time Programmable Read Only Memory (OTP-ROM) within it. It provides a PROTECTION bit to prevent intrusion of user's code in the OTP memory as well as 15 OPTION bits to match user's requirements.

With its OTP-ROM feature, the EM78P153S offers users a convenient way of developing and verifying their programs. Moreover, user developed code can be easily programmed with the ELAN writer.

2. FEATURES

• 14-lead packages : EM78P153S

• Operating voltage range : 2.3V~5.5V

• Available in temperature range: 0°C~70°C

• Operating frequency rang (base on 2 clocks):

  * Crystal mode: DC~20MHz at 5V, DC~8MHz at 3V, DC~4MHz at 2.3V.

  * ERC mode: DC~4MHz at 5V, DC~4MHz at 3V, DC~4MHz at 2.3V.

• Low power consumption:

  * less then 1.5 mA at 5V/4MHz

  * typical of 15 μA, at 3V/32KHz

  * typical of 1μA, during the sleep mode

• 1024 × 13 bits on chip ROM

• Built-in calibrated IRC oscillators (8MHz, 4MHz, 1MHz, 455KHz)

• Programmable prescaler of oscillator set-up time

• One security register to prevent the code in the OTP memory from intruding

• One configuration register to match the user's requirements

• 32× 8 bits on chip registers (SRAM, general purpose register)

• 2 bi-directional I/O ports

• 5 level stacks for subroutine nesting

• 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges, and with overflow interrupt

• Power down mode (SLEEP mode)

• Three available interruptions

  * TCC overflow interrupt

  * Input-port status changed interrupt (wake up from the sleep mode)

  * External interrupt

• Programmable free running watchdog timer

• 7 programmable pull-high I/O pins

• 7 programmable open-drain I/O pins

• 6 programmable pull-down I/O pins

• Two clocks per instruction cycle

• Package type: 14 pins SOP, DIP

  * 14 pin DIP 300mil: EM78P153SP

* 14 pin SOP 150mil: EM78P153SN

• The transient point of system frequency between HXT and LXT is around 400KHz.

3. PIN ASSIGNMENTS

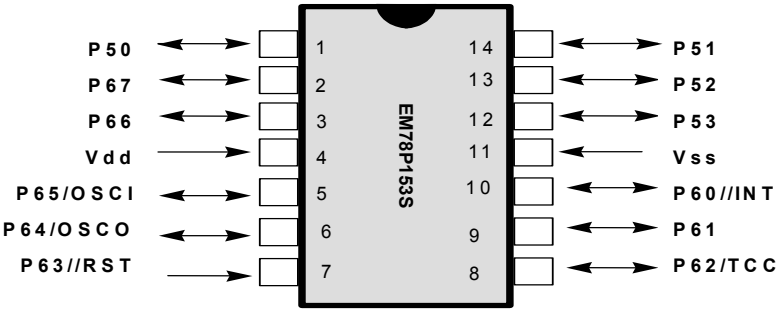

Fig. 1 Pin assignment

Table 1 Pin description

Symbol	Pin No.	Type	Function
Vdd	4	-	Power supply.
P65/OSCI	5	I/O	* General purpose I/O pin. * External clock signal input. * Input pin of XT oscillator. * Pull-high/open-drain * Wake up from sleep mode when the status of the pin changes.
P64/OSCO	6	I/O	* General purpose I/O pin. * External clock signal input. * Input pin of XT oscillator. * Pull-high/open-drain * Wake up from sleep mode when the status of the pin changes.
P63//RESET	7	I	* If set as /RESET and remain at logic low, the device will be under reset. * Wake up from sleep mode when the status of the pin changes. * Voltage on /RESET must not exceed Vdd during the normal mode. * Internal Pull-high is on if defined as /RESET. * P63 is input pin only
P62/TCC	8	I/O	* General purpose I/O pin. * Pull-high/open-drain/pull-down. * Wake up from sleep mode when the status of the pin changes. * External Timer/Counter input.
P61	9	I/O	* General purpose I/O pin. * Pull-high/open-drain/pull-down. * Wake up from sleep mode when the status of the pin changes. * Schmitt Trigger input during the programming mode
P60//INT	10	I/O	* General purpose I/O pin. * Pull-high/open-drain/pull-down. * Wake up from sleep mode when the status of the pin changes. * Schmitt Trigger input during the programming mode. * External interrupt pin triggered by falling edge.
P66, P67	2, 3	I/O	* General purpose I/O pin.

			* Pull-high/open-drain. * Wake up from sleep mode when the status of the pin changes.
P50~P53	1,14~13	I/O	* General purpose I/O pin. * Pull-down
P53	12	I/O	* General purpose I/O pin.
VSS	11	-	*Ground.