

## CD4001BC/CD4011BC

### Quad 2-Input NOR Buffered B Series Gate • Quad 2-Input NAND Buffered B Series Gate

#### General Description

The CD4001BC and CD4011BC quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to  $V_{DD}$  and  $V_{SS}$ .

#### Features

- Low power TTL:
  - Fan out of 2 driving 74L compatibility: or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1  $\mu$ A at 15V over full temperature range

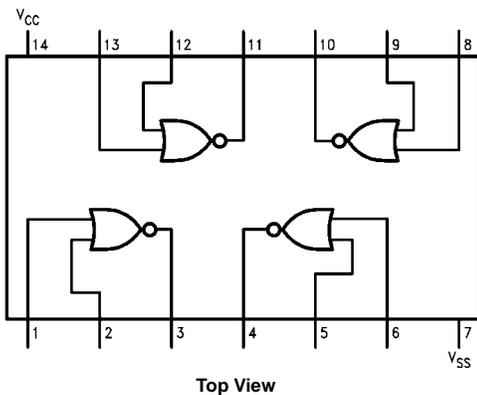
#### Ordering Code:

Order Number	Package Number	Package Description
CD4001BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4001BCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4001BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4011BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4011BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

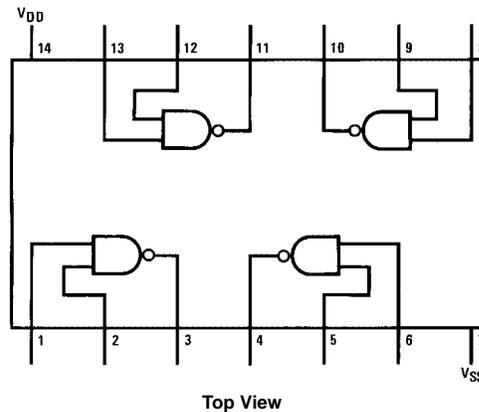
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagrams

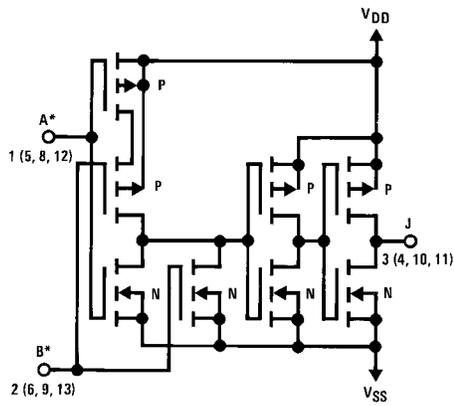
Pin Assignments for DIP, SOIC and SOP  
CD4001BC



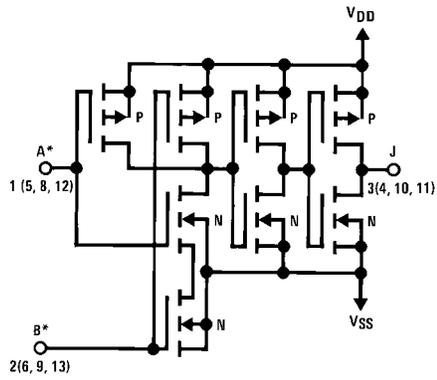
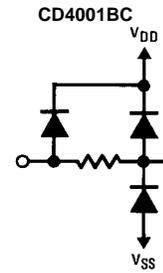
Pin Assignments for DIP and SOIC  
CD4011BC



Schematic Diagrams



$1/4$  of device shown  
 $J = \overline{A + B}$   
 Logical "1" = HIGH  
 Logical "0" = LOW  
 All inputs protected by standard  
 CMOS protection circuit.



$1/4$  of device shown  
 $J = \overline{A \cdot B}$   
 Logical "1" = HIGH  
 Logical "0" = LOW  
 All inputs protected by standard  
 CMOS protection circuit.

