



STW12NK90Z

N-channel 900 V, 0.72 Ω , 11 A TO-247
Zener-protected SuperMESH™ Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on) max}	I _D	P _w
STW12NK90Z	900 V	< 0.88 Ω	11 A	230 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Very good manufacturing repeatability

Application

- Switching applications

Description

This device is made using the SuperMESH™ Power MOSFET technology that is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

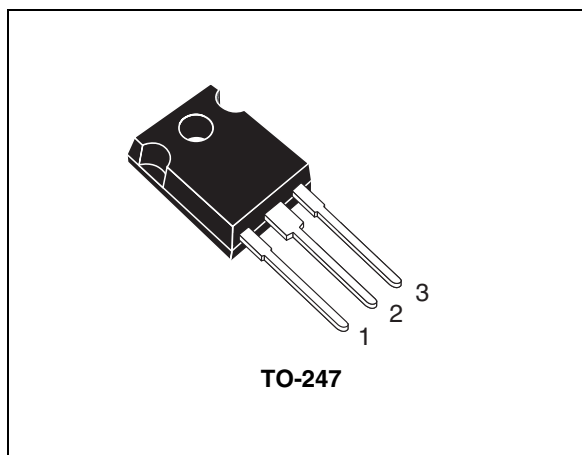


Figure 1. Internal schematic diagram

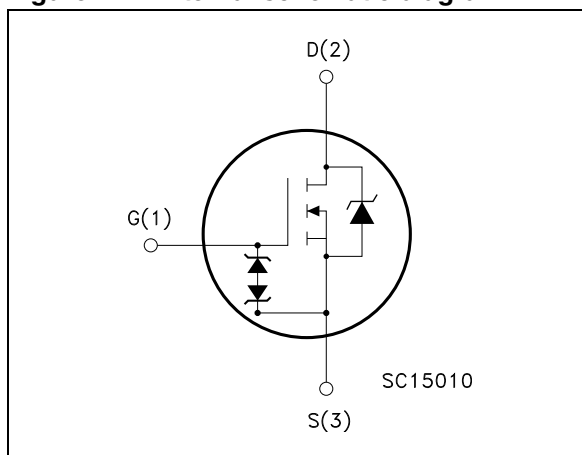


Table 1. Device summary

Order code	Marking	Package	Packaging
STW12NK90Z	W12NK90Z	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	900	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	11	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	44	A
P_{tot}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	230	W
	Derating Factor	1.85	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100 pF, R=1.5 k Ω)	6000	V
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 11\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.54	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
T_J	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	11	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	500	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	900			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$, $T_C = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$		0.72	0.88	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 5.5\text{ A}$	-	11		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	3500 280 58		pF pF pF
$C_{oss\ eq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }800\text{ V}$	-	117		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 450\text{ V}$, $I_D = 5\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14)	-	31 20 88 55		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 720\text{ V}$, $I_D = 10\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 4.7\text{ }\Omega$ (see Figure 15)	-	113 19 60	152	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. $C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		11 44	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 10\text{ A}$, $V_{DD} = 50\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 16)	-	728 7.8 21.6		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 10\text{ A}$, $V_{DD} = 50\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16)	-	964 11 23		ns μC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.