STEREO DIGITAL AMPLIFIER POWER STAGE

FEATURES

- **2×125 W at 10% THD+N Into 4-Ω BTL**
- **2×98 W at 10% THD+N Into 6-Ω BTL**
- **2×76 W at 10% THD+N Into 8-Ω BTL**
- **4×45 W at 10% THD+N Into 3-Ω SE**
- **4×35 W at 10% THD+N Into 4-Ω SE**
- **1×192 W at 10% THD+N Into 3-Ω PBTL**
- **1×240 W at 10% THD+N Into 2-Ω PBTL**
- **>100-dB SNR (A-Weighted)**
- **<0.1% THD+N at 1 W**
- **Thermally Enhanced Package Option:**
  - **DKD (36-Pin PSOP3)**
- **High-Efficiency Power Stage (>90%) With 140-mΩ Output MOSFETs**
- **Power-On Reset for Protection on Power Up Without Any Power-Supply Sequencing**
- **Integrated Self-Protection Circuits Including:**
  - **Undervoltage**
  - **Overtemperature**
  - **Overload**
  - **Short Circuit**
- **Error Reporting**
- **EMI Compliant When Used With Recommended System Design**
- **Intelligent Gate Drive**

APPLICATIONS

- **Mini/Micro Audio System**
- **DVD Receiver**
- **Home Theater**

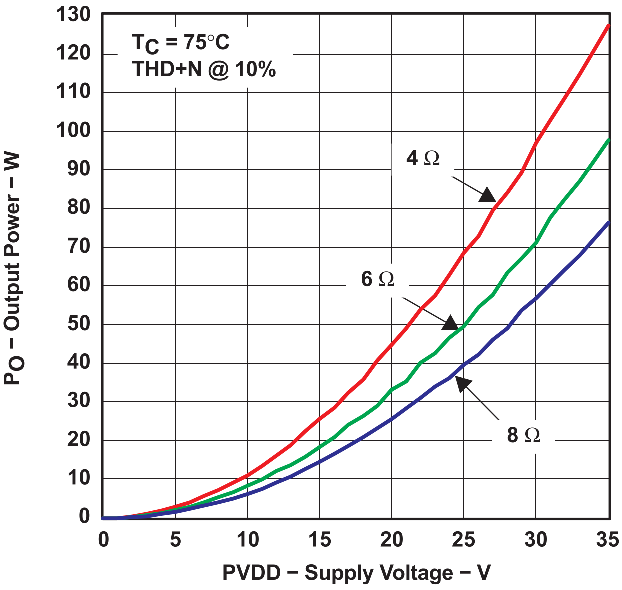
DESCRIPTION

The TAS5152 is a third-generation, high-performance, integrated stereo digital amplifier power stage with improved protection system. The TAS5152 is capable of driving a 4-Ω bridge-tied load (BTL) at up to 125 W per channel with low integrated noise at the output, low THD+N performance, and low idle power dissipation.

A low-cost, high-fidelity audio system can be built using a TI chipset, comprised of a modulator (e.g., TAS5508) and the TAS5152. This system only requires a simple passive LC demodulation filter to deliver high-quality, high-efficiency audio amplification with proven EMI compliance. This device requires two power supplies, 12 V for GVDD and VDD, and 35 V for PVDD. The TAS5152 does not require power-up sequencing due to internal power-on reset. The efficiency of this digital amplifier is greater than 90% into 6 Ω, which enables the use of smaller power supplies and heatsinks.

The TAS5152 has an innovative protection system integrated on-chip, safeguarding the device against a wide range of fault conditions that could damage the system. These safeguards are short-circuit protection, overcurrent protection, undervoltage protection, and overtemperature protection. The TAS5152 has a new proprietary current-limiting circuit that reduces the possibility of device shutdown during high-level music transients. A new programmable overcurrent detector allows the use of lower-cost inductors in the demodulation output filter.

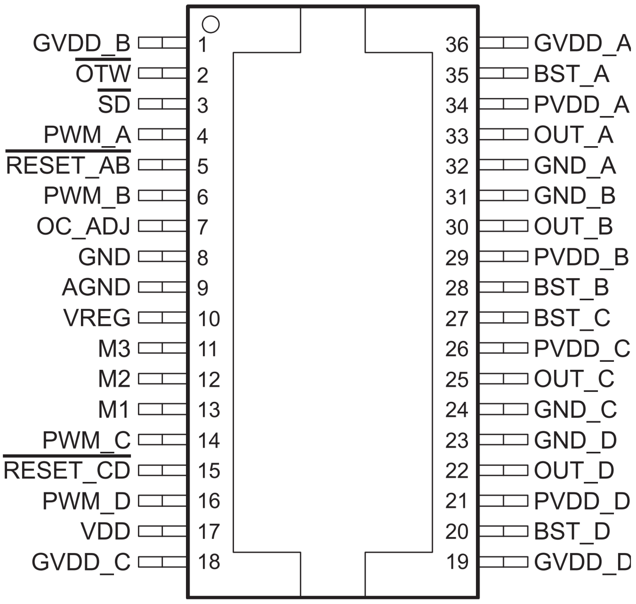
BTL OUTPUT POWER vs SUPPLY VOLTAGE



GENERAL INFORMATION

The TAS5152 is available in a 36-pin PSOP3 (DKD) thermally enhanced package. The package contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heatsink.

DKD PACKAGE
(TOP VIEW)



MODE Selection Pins

MODE PINS			PWM INPUT	OUTPUT CONFIGU-RATION	PROTECTION SCHEME
M3	M2	M1			
0	0	0	2N (1) AD/BD modulation	2 channels BTL output	BTL mode (2)
0	0	1	Reserved		
0	1	0	1N (1) AD modulation	2 channels BTL output	BTL mode (2)
0	1	1	1N (1) AD modulation	1 channel PBTL output	PBTL mode. Only PWM_A input is used.
1	0	0	1N (1) AD modulation	4 channels SE output	Protection works similarly to BTL mode (2). Only difference in SE mode is that OUT_x is Hi-Z instead of a pulldown through internal pulldown resistor.
1	0	1	Reserved		
1	1	0			
1	1	1			

(1) The 1N and 2N naming convention is used to indicate the required number of PWM lines to the power stage per channel in a specific mode.

(2) An overload protection (OLP) occurring on A or B causes both channels to shut down. An OLP on C or D works similarly. Global errors like overtemperature error (OTE), undervoltage protection (UVP) and power-on reset (POR) affect all channels.

Package Heat Dissipation Ratings (1)

PARAMETER	TAS5152DKD
$R_{\theta JC}$ (°C/W)—2 BTL or 4 SE channels (8 transistors)	1.28
$R_{\theta JC}$ (°C/W)—1 BTL or 2 SE channel(s) (4 transistors)	2.56
$R_{\theta JC}$ (°C/W)—(1 transistor)	8.6
Pad area (2)	80 mm^2

(1) JC is junction-to-case, CH is case-to-heatsink.

(2) $R_{\theta CH}$ is an important consideration. Assume a 2-mil thickness of typical thermal grease between the pad area and the heatsink. The $R_{\theta CH}$ with this condition is 0.8°C/W for the DKD package and 1.8°C/W for the DDV package.

Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

TAS5152	
VDD to AGND	–0.3 V to 13.2 V
GVDD_X to AGND	–0.3 V to 13.2 V
PVDD_X to GND_X (2)	–0.3 V to 50 V
OUT_X to GND_X (2)	–0.3 V to 50 V
BST_X to GND_X (2)	–0.3 V to 63.2 V
VREG to AGND	–0.3 V to 4.2 V
GND_X to GND	–0.3 V to 0.3 V
GND_X to AGND	–0.3 V to 0.3 V
GND to AGND	–0.3 V to 0.3 V
PWM_X, OC_ADJ, M1, M2, M3 to AGND	–0.3 V to 4.2 V
$\overline{\text{RESET\_X}}$, $\overline{\text{SD}}$, $\overline{\text{OTW}}$ to AGND	–0.3 V to 7 V
Maximum continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW}}$)	9 mA
Maximum operating junction temperature range, T_J	0°C to 125°C
Storage temperature	–40°C to 125°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Minimum pulse width low	50 ns

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

Ordering Information

T_A	PACKAGE	DESCRIPTION
0°C to 70°C	TAS5152DKD	36-pin PSOP3

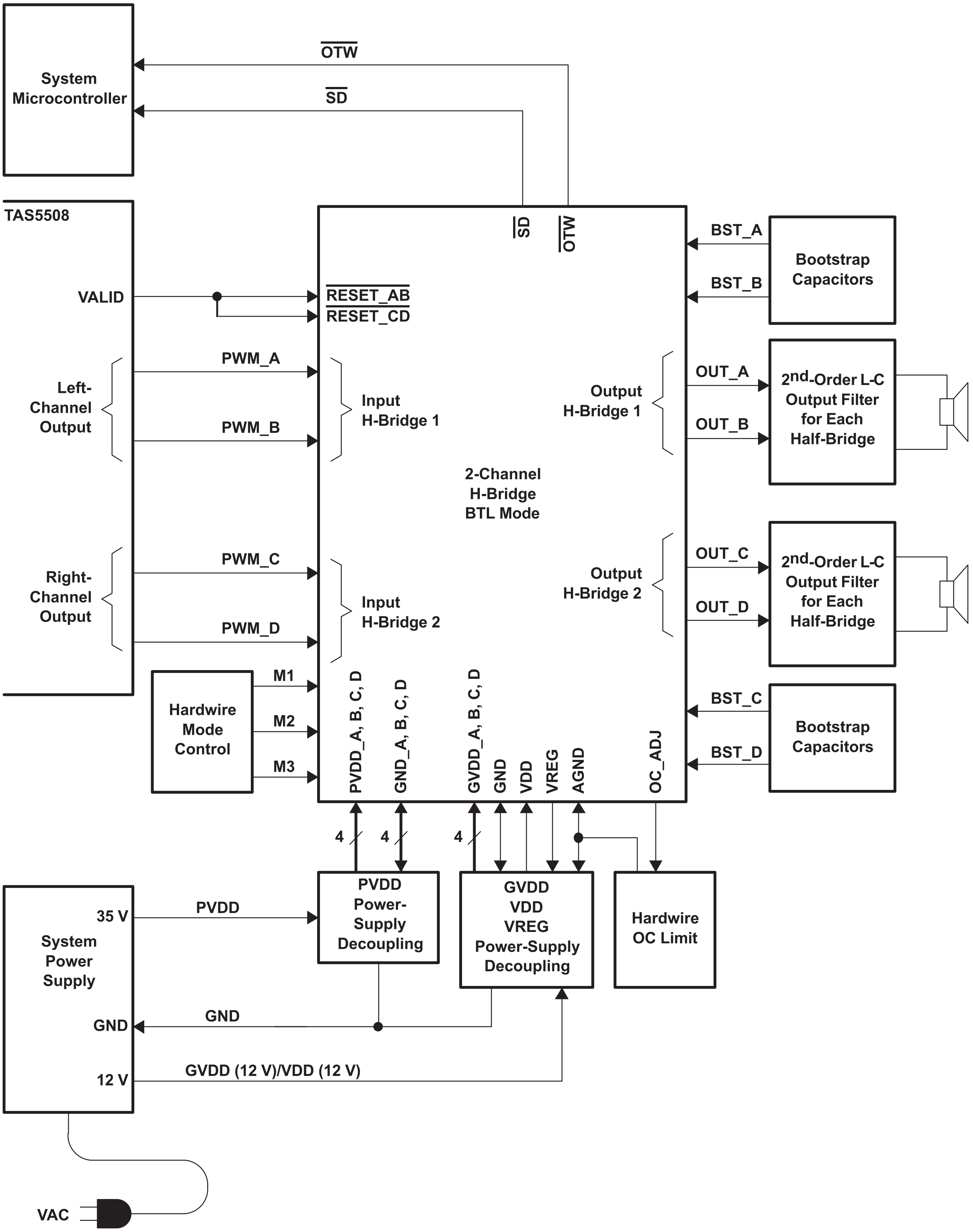
For the most current specification and package information, see the TI Web site at www.ti.com.

Terminal Functions

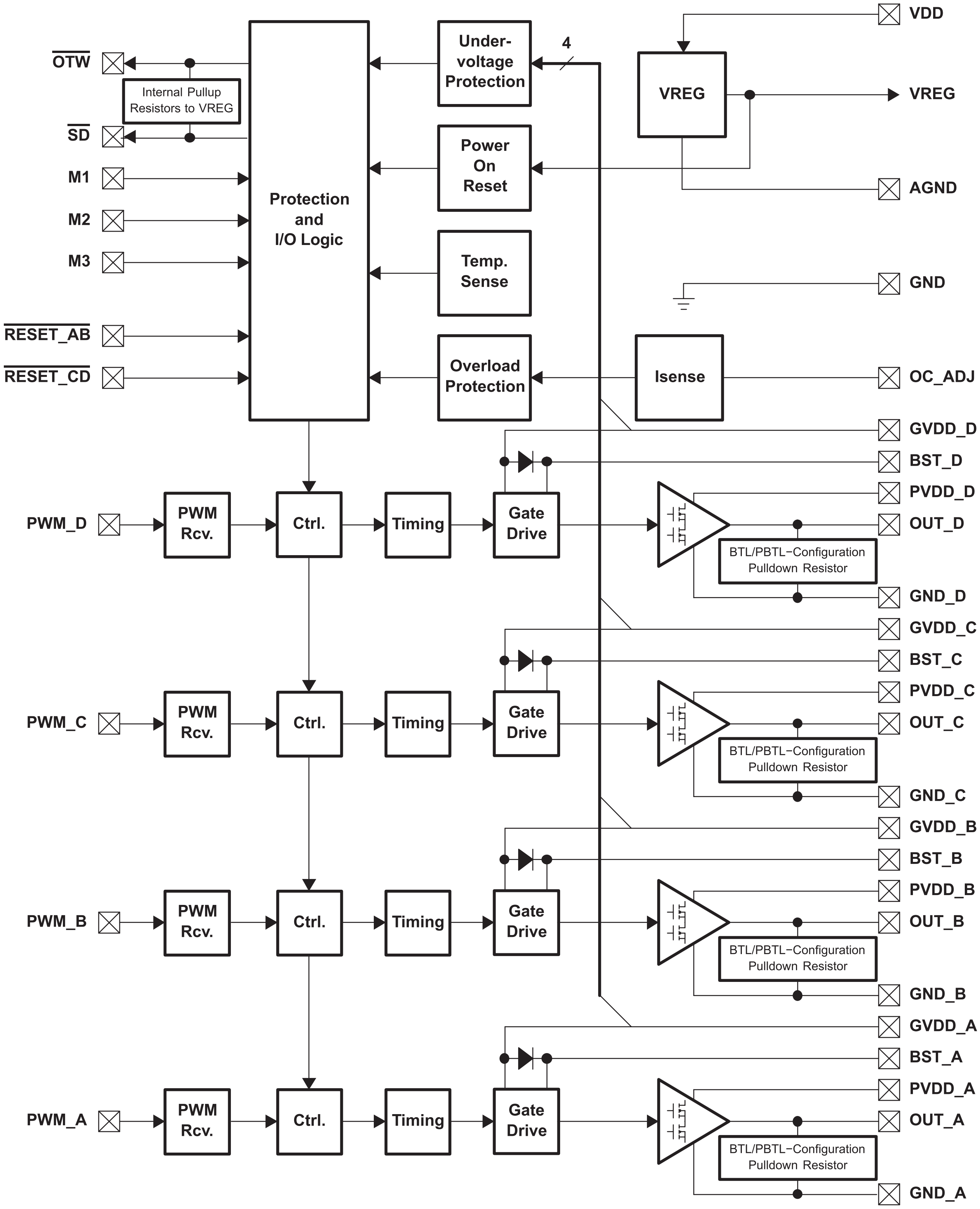
TERMINAL		FUNCTION (1)	DESCRIPTION
NAME	NO.		
AGND	9	P	Analog ground
BST_A	35	P	HS bootstrap supply (BST), external capacitor to OUT_A required
BST_B	28	P	HS bootstrap supply (BST), external capacitor to OUT_B required
BST_C	27	P	HS bootstrap supply (BST), external capacitor to OUT_C required
BST_D	20	P	HS bootstrap supply (BST), external capacitor to OUT_D required
GND	8	P	Ground
GND_A	32	P	Power ground for half-bridge A
GND_B	31	P	Power ground for half-bridge B
GND_C	24	P	Power ground for half-bridge C
GND_D	23	P	Power ground for half-bridge D
GVDD_A	36	P	Gate-drive voltage supply requires 0.1-µF capacitor to AGND
GVDD_B	1	P	Gate-drive voltage supply requires 0.1-µF capacitor to AGND
GVDD_C	18	P	Gate-drive voltage supply requires 0.1-µF capacitor to AGND
GVDD_D	19	P	Gate-drive voltage supply requires 0.1-µF capacitor to AGND
M1	13	I	Mode selection pin
M2	12	I	Mode selection pin
M3	11	I	Mode selection pin
OC_ADJ	7	O	Analog overcurrent programming pin requires resistor to ground
$\overline{\text{OTW}}$	2	O	Overtemperature warning signal, open drain, active-low
OUT_A	33	O	Output, half-bridge A
OUT_B	30	O	Output, half-bridge B
OUT_C	25	O	Output, half-bridge C
OUT_D	22	O	Output, half-bridge D
PVDD_A	34	P	Power-supply input for half-bridge A requires close decoupling of 0.1-µF capacitor to GND_A
PVDD_B	29	P	Power-supply input for half-bridge B requires close decoupling of 0.1-µF capacitor to GND_B
PVDD_C	26	P	Power-supply input for half-bridge C requires close decoupling of 0.1-µF capacitor to GND_C
PVDD_D	21	P	Power-supply input for half-bridge D requires close decoupling of 0.1-µF capacitor to GND_D
PWM_A	4	I	Input signal for half-bridge A
PWM_B	6	I	Input signal for half-bridge B
PWM_C	14	I	Input signal for half-bridge C
PWM_D	16	I	Input signal for half-bridge D
$\overline{\text{RESET\_AB}}$	5	I	Reset signal for half-bridge A and half-bridge B, active-low
$\overline{\text{RESET\_CD}}$	15	I	Reset signal for half-bridge C and half-bridge D, active-low
$\overline{\text{SD}}$	3	O	Shutdown signal, open drain, active-low
VDD	17	P	Power supply for digital voltage regulator requires 0.1-µF capacitor to GND.
VREG	10	P	Digital regulator supply filter pin requires 0.1-µF capacitor to AGND

(1) I = input, O = Output, P = Power

SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



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