5A, 32V, 500kHz Step-Down Converter

General Description

The RT8289 is a step-down regulator with an internal Power MOSFET. It achieves 5A of continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization.

The RT8289 prorides protections such as cycle-by-cycle current limiting and thermal shutdown. In shutdown mode, the regulator draws 25A of supply current.

The RT8289 requires a minimum number of external components, to proride a compact solution.

The RT8289 is available in a SOP-8 (Exposed Pad) package.

Ordering Information

RT8289 □□

Package Type
SP : SOP-8 (Exposed Pad-Option 1)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current require-ments of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

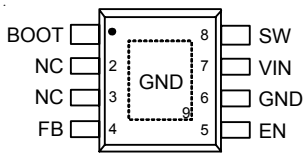
- **High Output Current up to 5A**
- **Internal Soft-Start**
- **100mΩ Internal Power MOSFET Switch**
- **Internal Compensation Minimizes External Parts Count**
- **High Efficiency up to 90%**
- **25μA Shutdown Current**
- **Fixed 500kHz Frequency**
- **Thermal Shutdown Protection**
- **Cycle-by-Cycle Over Current Protection**
- **Wide 5.5V to 32V Operating Input Range**
- **Adjustable Output Voltage from 1.222V to 26V**
- **Available in an SOP-8 (Exposed Pad) Package**
- **RoHS Compliant and Halogen Free**

Applications

- Distributive Power Systems
- LCD TV
- DSL Modems
- Pre-regulator for Linear Regulators
- Battery Charger

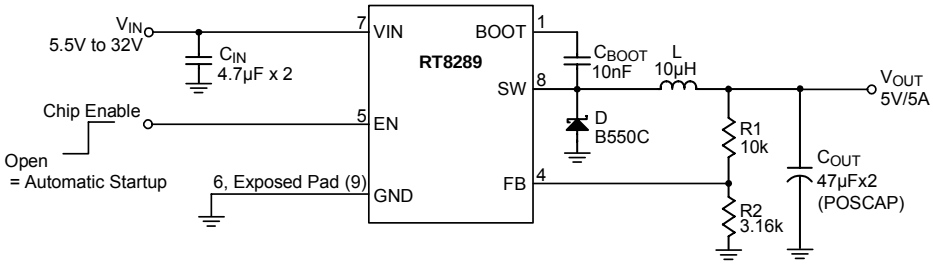
Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

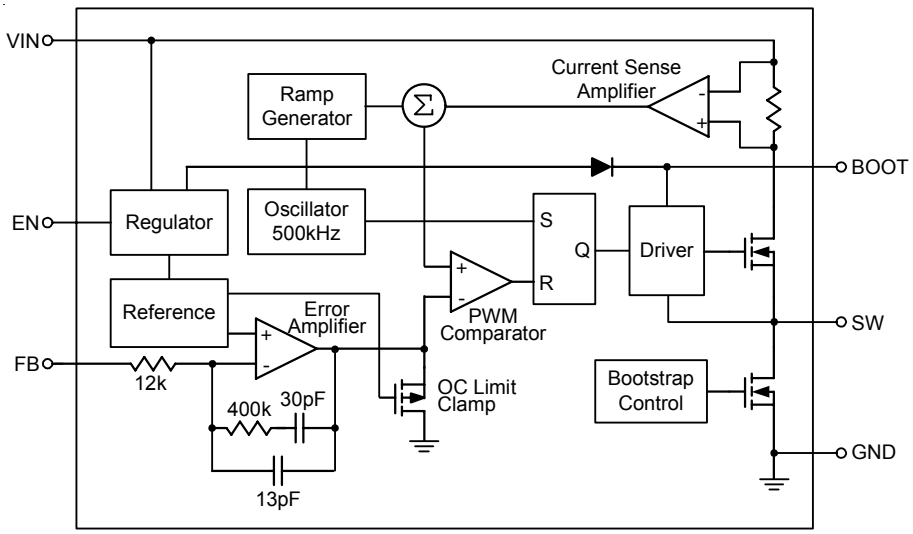
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	High Side Gate Drive Bootstrap Input. BOOT supplies the drive for the high side N-MOSFET switch. Connect a 10nF or greater capacitor from SW to BOOT to power the high side switch.
2, 3	NC	No Internal Connection.
4	FB	Feedback Input. FB senses the output voltage to regulate said voltage. Drive FB with a resistive voltage divider from the output voltage. The value of the divider resistors also sets loop bandwidth. The feedback threshold is 1.222V.
5	EN	Chip Enable (Active High). EN is a digital input that turns the regulator on or off. Drive EN higher than 1.4V to turn on the regulator, lower than 0.4V to turn it off. For automatic startup, leave EN unconnected.
6, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	VIN	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive V_{IN} with a 5.5V to 32V power source. Bypass V_{IN} to GND with a suitably large capacitor to eliminate noise on the input to the IC.
8	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BOOT to power the high side switch.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{IN} ---- 0.3V to 34V
- Switching Voltage, SW (Note 2) ---- –0.6V to (V_{IN} + 0.3V)
- BOOT Voltage ---- (V_{SW} – 0.3V) to (V_{SW} + 6V)
- Other Pins Voltage ---- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---- 1.333W
- Package Thermal Resistance (Note 3)
  SOP-8 (Exposed Pad), θ_{JA} ---- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---- 15°C/W
- Junction Temperature ---- 150°C
- Lead Temperature (Soldering, 10 sec.) ---- 260°C
- Storage Temperature Range ---- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Mode) ---- 2kV
  MM (Machine Mode) ---- 200V

Recommended Operating Conditions (Note 5)

- Supply Voltage, V_{IN} ---- 5.5V to 32V
- Enable Voltage, V_{EN} ---- 0V to 5.5V
- Junction Temperature Range ---- –40°C to 125°C
- Ambient Temperature Range ---- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Reference Voltage		V_{FB}	5.5V ≦ V_{IN} ≦ 32V	1.202	1.222	1.239	V
High Side Switch-On Resistance		$R_{DS(ON)1}$		--	100	--	mΩ
Low Side Switch-On Resistance		$R_{DS(ON)2}$		--	10	--	Ω
Upper Switch Leakage			V_{EN} = 0V, V_{SW} = 0V	--	0	10	μA
Current Limit		I_{LIM}	Duty = 90%; $V_{BOOT-SW}$ = 4.8V	--	6.8	--	A
Current Sense Transconductance		G_{CS}	Output Current to V_{COMP}	--	5.5	--	A/V
Oscillator Frequency		f_{SW}		--	500	--	kHz
Short Circuit Oscillation Frequency			V_{FB} = 0V	--	120	--	kHz
Maximum Duty Cycle		D_{MAX}	V_{FB} = 1V	--	90	--	%
Minimum On-Time		t_{ON}		--	100	--	ns
Under Voltage Lockout Threshold Rising				--	4.2	--	V
Under Voltage Lockout Threshold Hysteresis				--	200	--	mV
En Threshold	Logic Low Voltage	V_{IL}		--	--	0.4	V
	Logic High Voltage	V_{IH}		1.4	--	5.5	
Enable Pull Up Current				--	1	--	μA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	25	--	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 1.5V	--	0.8	1	mA
Soft-Start Period			--	4	--	ms
Thermal Shutdown	T_{SD}		--	150	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. The low side MOSFET body diode forward current must be lower than 1mA

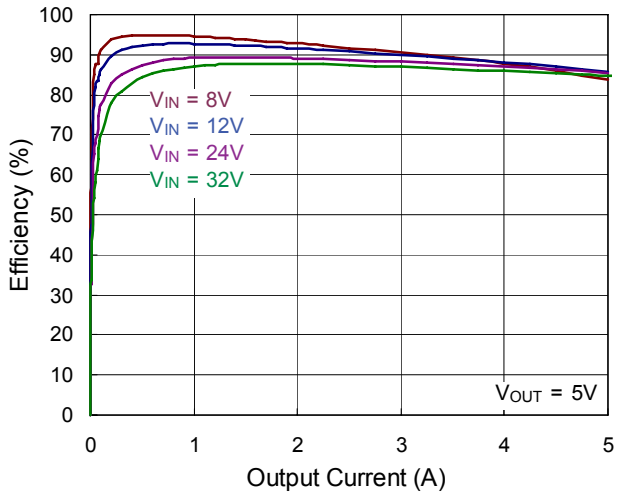
Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precaution is recommended.

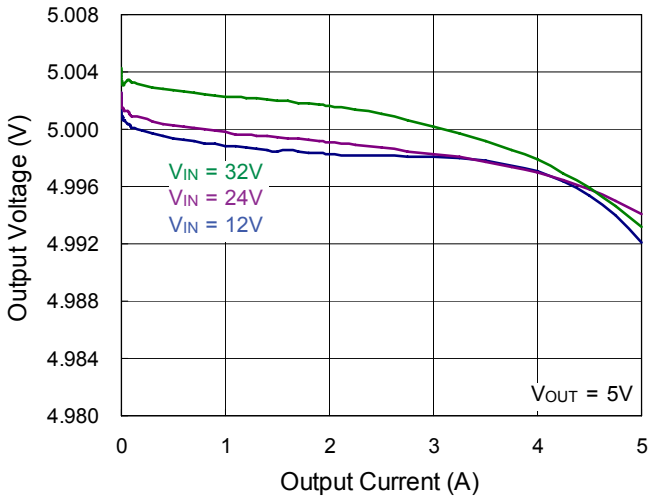
Note 5. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

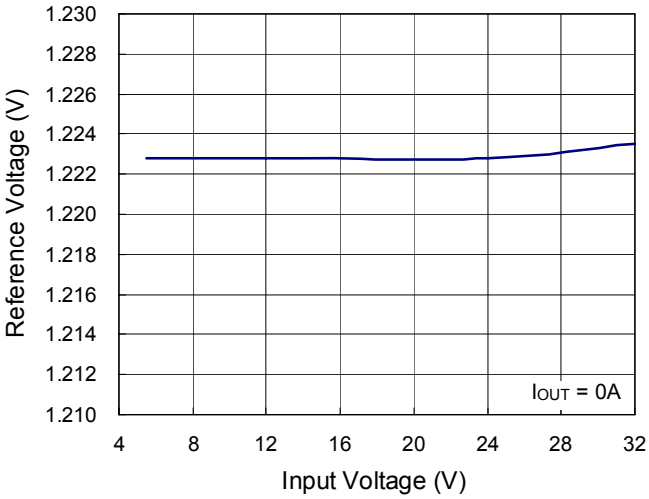
Efficiency vs. Output Current



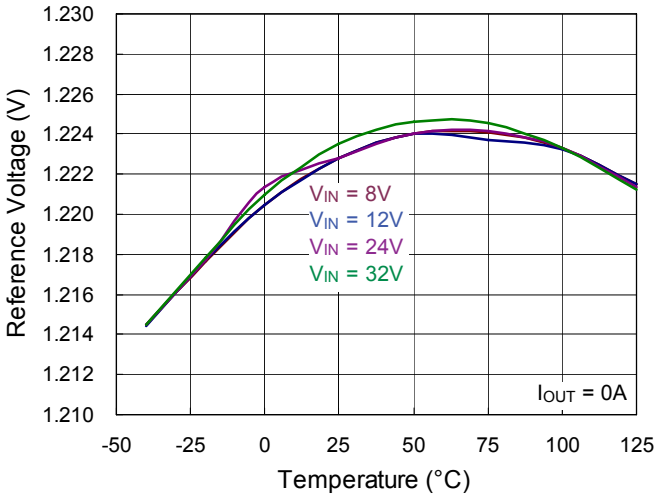
Output Voltage vs. Output Current



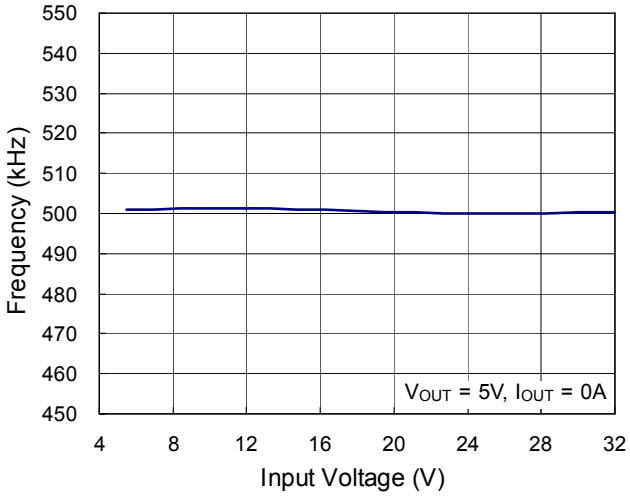
Reference Voltage vs. Input Voltage



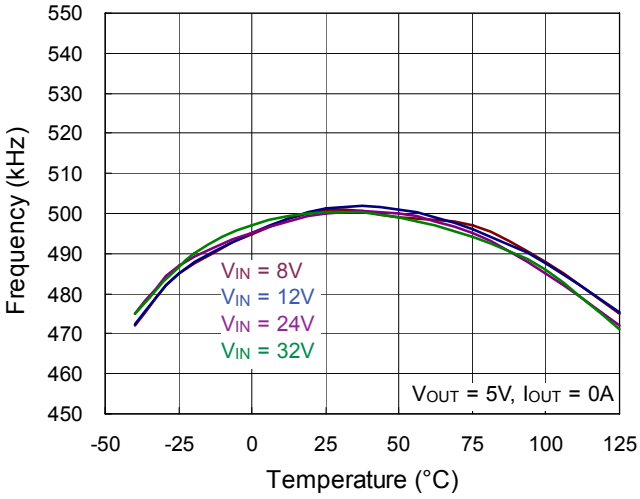
Reference Voltage vs. Temperature



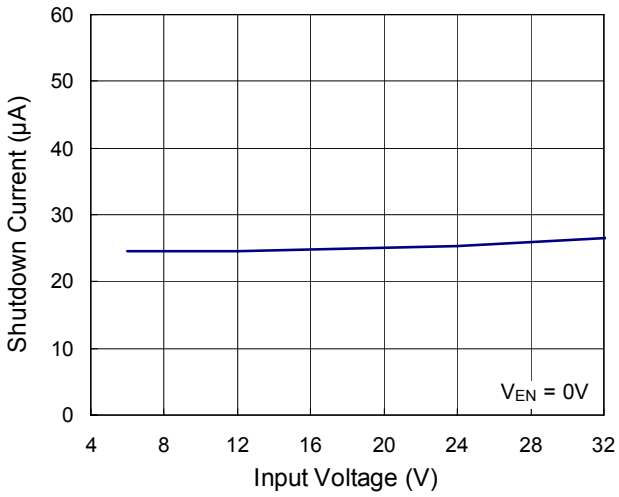
Frequency vs. Input Voltage



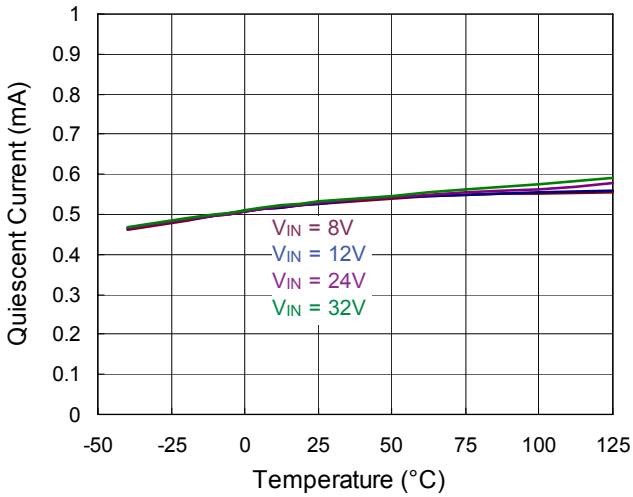
Frequency vs. Temperature



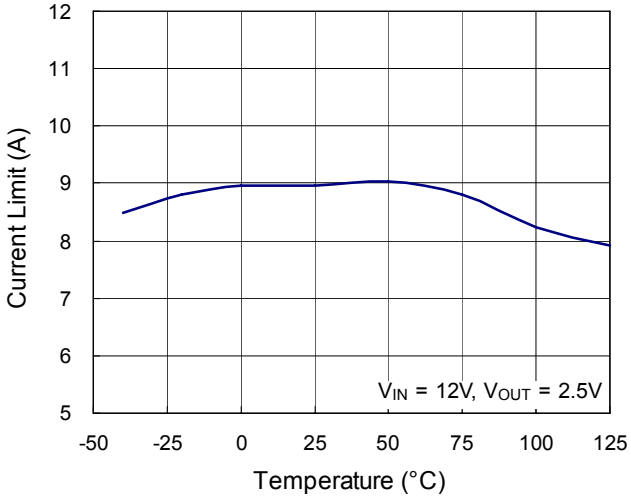
Shutdown Current vs. Input Voltage



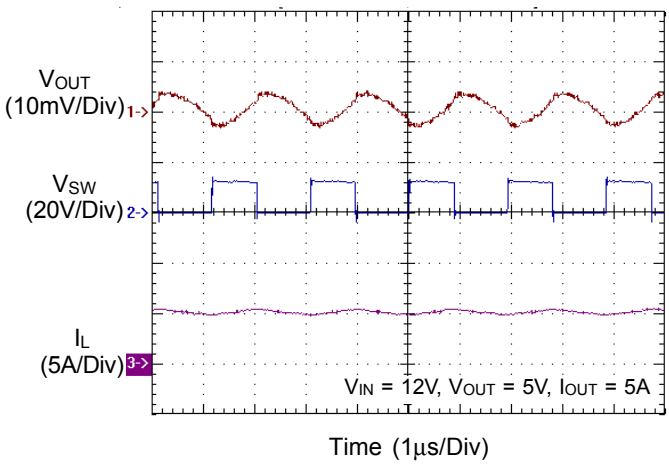
Quiescent Current vs. Temperature



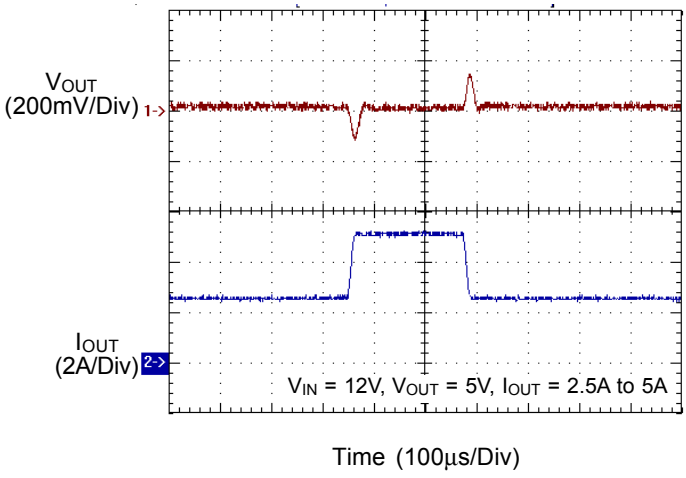
Current Limit vs. Temperature



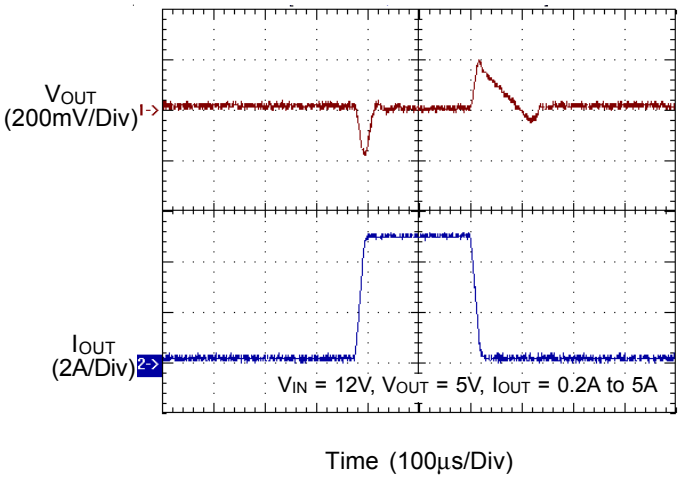
Switching



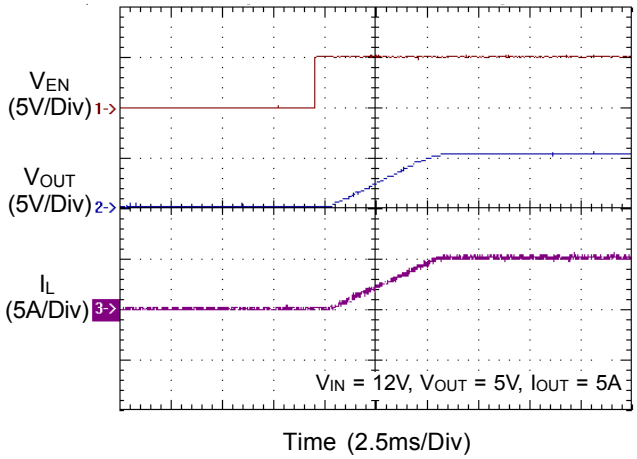
Load Transient Response



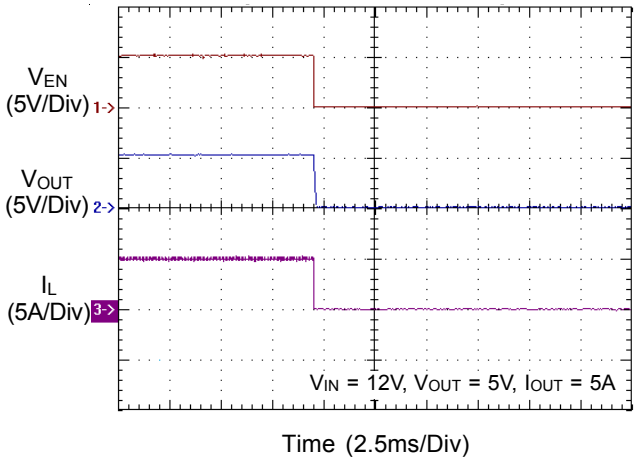
Load Transient Response



Power On from EN



Power Off from EN



Application Information

The RT8289 is an asynchronous high voltage buck converter that can support the input voltage range from 5.5V to 32V and the output current can be up to 5A.

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

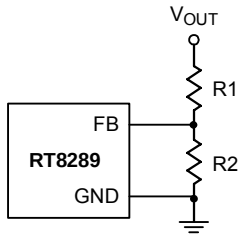


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

Where V_{FB} is the feedback reference voltage (1.222V typ.).

Where R1 = 10kΩ.

External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT8289.

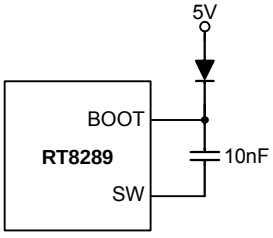


Figure 2. External Bootstrap Diode

Soft-Start

The RT8289 contains an in ternal soft-start clamp that gradually raises the output voltage. The typical soft-start time is 4ms.

Chip Enable Operation

The EN pin is the chip enable input. Pull the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT8289 quiescent current drops to lower than 25μA. Drive the EN pin to high (>1.4V, < 5.5V) will turn on the device again. If the EN pin is open, it will be pulled to high by internal circuit.For external timing control (e.g.RC),the EN pin can also be externally pulled to High by adding a 100kΩ or greater resistor from the VIN pin (see Figure 3).

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1-\frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.2(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1-\frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TAIYO YUDEN	NR10050	10 x 9.8 x 5
TDK	SLF12565	12.5 x 12.5 x 6.5

Diode Selection

When the power switch turns off, the path for the current is through the diode connected between the switch output and ground. This forward biased diode must have a minimum voltage drop and recovery times. Schottky diode is recommended and it should be able to handle those current. The reverse voltage rating of the diode should be greater than the maximum input voltage, and current rating should be greater than the maximum load current. For more detail please refer to Table 4.

C_{IN} and C_{OUT} Selection

The input capacitance, $C_{IN,}$ is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor,two 4.7μF low ESR ceramic capacitors are recommended. For the recommended capacitor, please refer to table 3 for more detail.

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this

recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on SW pin when high side MOSFET is turned-on/off, this spike voltage on SW may impact on EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One is to place an R-C snubber between SW and GND and make them as close as possible to the SW pin (see Figure 3). Another method is to add a resistor in series with the bootstrap capacitor, C_{BOOT}. But this method will decrease the driving capability to the high side MOSFET. It is strongly recommended to reserve the R-C snubber during PCB layout for EMI improvement. Moreover, reducing the SW trace area and keeping the main power in a small loop will be helpful on EMI performance. For detailed PCB layout guide, please refer to the section of Layout Consideration.

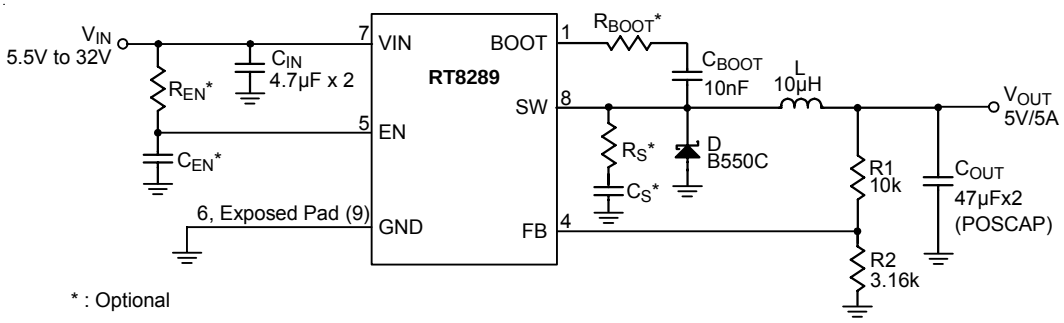


Figure 3. Reference Circuit with Snubber and Enable Timing Control

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8289, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For PSOP-8 package, the thermal resistance θ_{JA} is 75°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$P_{D(MAX)}$ = (125°C − 25°C) / (75°C/W) = 1.333W (min.copper area PCB layout)

$P_{D(MAX)}$ = (125°C − 25°C) / (49°C/W) = 2.04W (70mm^2 copper area PCB layout)

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 4, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 4a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 4.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm^2 (Figure 4.e) reduces the θ_{JA} to 49°C/W.

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J\ (MAX)}$ and thermal resistance θ_{JA}. For the RT8289, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

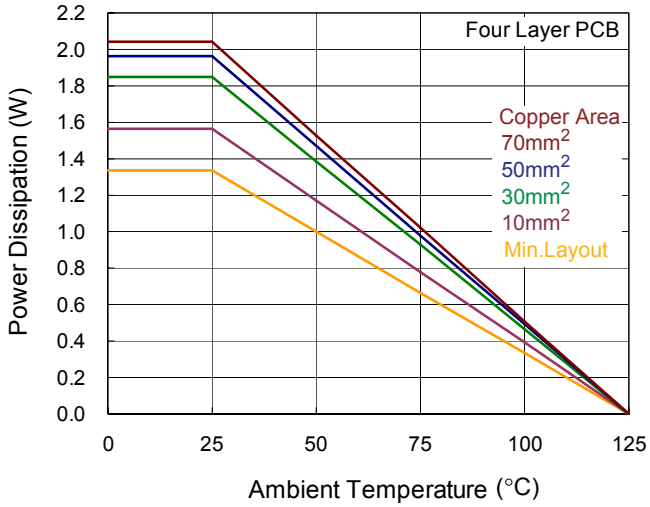
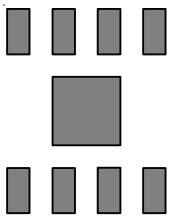
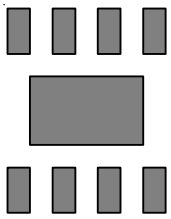


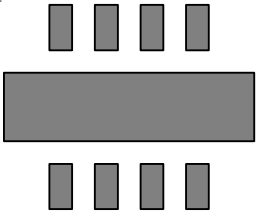
Figure 5. Derating Curves for RT8289 Package



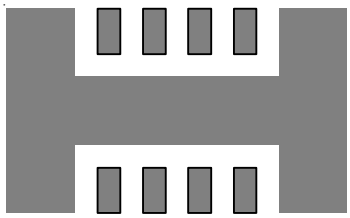
(a) Copper Area = (2.3 x 2.3) mm^2, θ_{JA} = 75°C/W



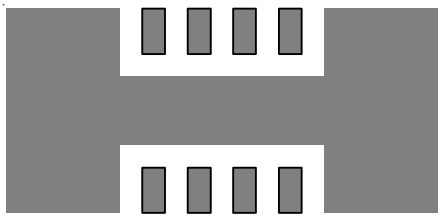
(b) Copper Area = $10mm^2$, θ_{JA} = 64°C/W



(c) Copper Area = $30mm^2$, θ_{JA} = 54°C/W



(d) Copper Area = $50mm^2$, θ_{JA} = 51°C/W



(e) Copper Area = $70mm^2$, θ_{JA} = 49°C/W

Figure 4. Themal Resistance vs. Copper Area Layout Design

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT8289.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8289.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.
- An example of PCB layout guide is shown in Figure 6 for reference.

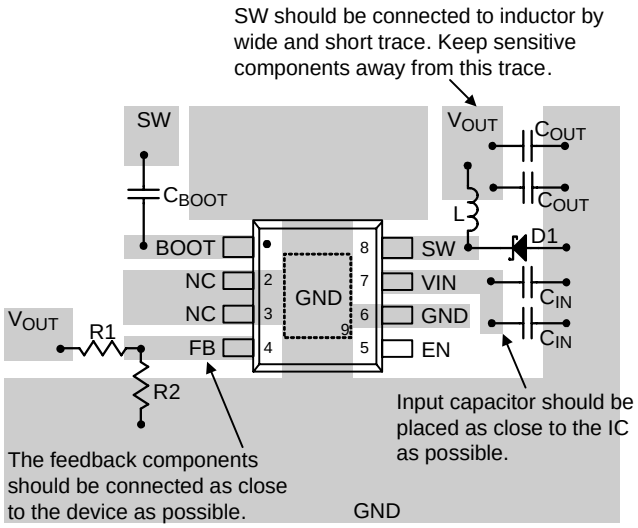


Figure 6. PCB Layout Guide

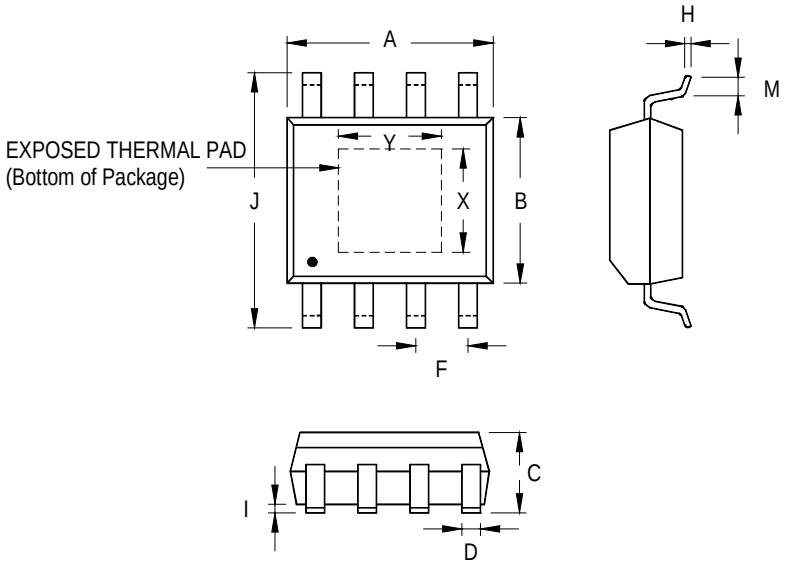
Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (μF)	Case Size
C_{IN}	MURATA	GRM32ER71H475K	4.7	1206
C_{IN}	TAIYO YUDEN	UMK325BJ475MM-T	4.7	1206
C_{OUT}	SANYO	16IQC47M	47	D2
C_{OUT}	SANYO	10TPE47MAIB	47	B2
C_{OUT}	MURATA	GRM31CR60J476M	47	1206

Table 4. Suggested Diode

Component Supplier	Series	V_{RRM} (V)	I_{OUT} (A)	Package
DIODES	B550C	50	5	SMC
PANJIT	SK55	50	5	SMC

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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