

## CMOS Low-Power Monostable/Astable Multivibrator

High Voltage Types (20-Volt Rating)

■ CD4047B consists of a gatatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, -TRIGGER, ASTABLE, ASTABLE, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, Q, and OSCILLATOR. In all modes of operation, and external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input or a low level on the ASTABLE input, or both. The period of the square wave at the Q and Q outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the ASTABLE input allow the circuit to be used as a gatatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

The CD4047B triggers in the monostable mode when a positive-going edge occurs on the +TRIGGER-input while the -TRIGGER is held low. Input pulses may be of any duration relative to the output pulse.

If retrigger capability is desired, the RETRIGGER input is pulsed. The retriggerable mode of operation is limited to positive-going edge. The CD4047B will retrigger as long as the RETRIGGER-input is high, with or without transitions (See Fig. 34).

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the ASTABLE input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. For monostable operation, whenever V<sub>DD</sub> is applied, an internal power-on reset circuit will clock the Q output low within one output period (t<sub>M</sub>).

The CD4047B-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- Low power consumption: special CMOS oscillator configuration
- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required
- Buffered inputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Monostable Multivibrator Features:

- Positive- or negative-edge trigger
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse width expansion
- Internal power-on reset circuit
- Long pulse widths possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

### Astable Multivibrator Features:

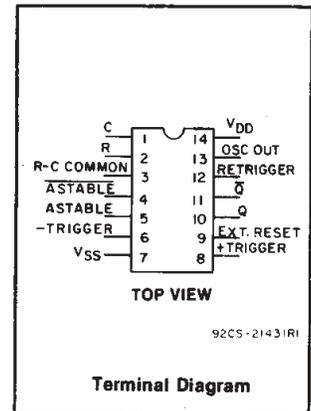
- Free-running or gatatable operating modes
- 50% duty cycle

- Oscillator output available
- Good astable frequency stability:  
Frequency deviation:  
= ±2% + 0.03%/°C @ 100 kHz  
= ±0.5% + 0.015%/°C @ 10 kHz  
(circuits "trimmed" to frequency V<sub>DD</sub> = 10 V ± 10%)

### Applications:

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- Envelope detection
- Frequency multiplication
- Frequency division
- Frequency discriminators
- Timing circuits
- Time-delay applications



### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range)	3	18	V

NOTE: IF AT 15 V OPERATION A 10 MΩ RESISTOR IS USED THE OPERATING TEMPERATURE SHOULD BE BETWEEN -25°C and 100°C

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> ) Voltages referenced to V <sub>SS</sub> Terminal	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V <sub>DD</sub> + 0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P <sub>D</sub> ): For T <sub>A</sub> = -55°C to +100°C	500mW
For T <sub>A</sub> = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

# CD4047B Types

## CD4047B FUNCTIONAL TERMINAL CONNECTIONS

NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲  
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V <sub>DD</sub>	TO V <sub>SS</sub>	INPUT TO		
Astable Multivibrator: Free Running	4,5,6,14	7,8,9,12	—	10,11,13	$t_A(10,11) = 4.40 RC$
True Gating	4,6,14	7,8,9,12	5	10,11,13	$t_A(13) = 2.20 RC^*$
Complement Gating	6,14	5,7,8,9,12	4	10,11,13	
Monostable Multivibrator: Positive-Edge Trigger	4,14	5,6,7,9,12	8	10,11	$t_M(10,11) = 2.48 RC$
Negative-Edge Trigger	4,8,14	5,7,9,12	6	10,11	
Retriggerable	4,14	5,6,7,9	8,12	10,11	
External Countdown*	14	5,6,7,8,9,12	—	10,11	

▲ See Text.

\* First positive 1/2 cycle pulse-width = 2.48 RC, see Note on Page 3-134.

\* Input Pulse to Reset of External Counting Chip External Counting Chip Output To Terminal 4

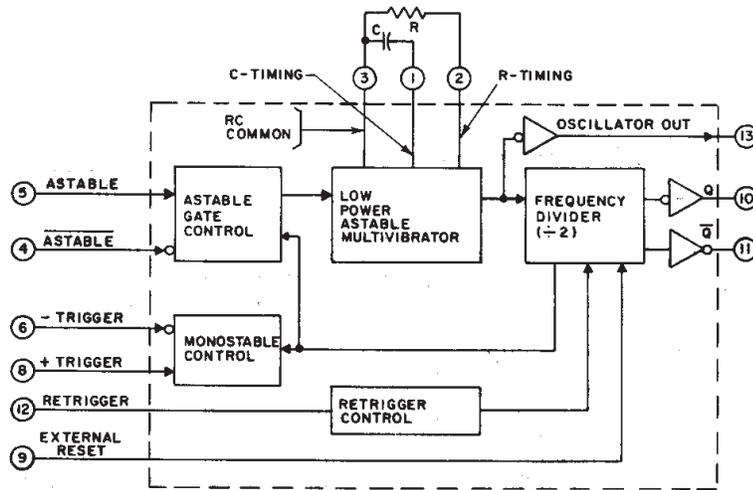


Fig. 1—CD4047B logic block diagram.

92CS-29071

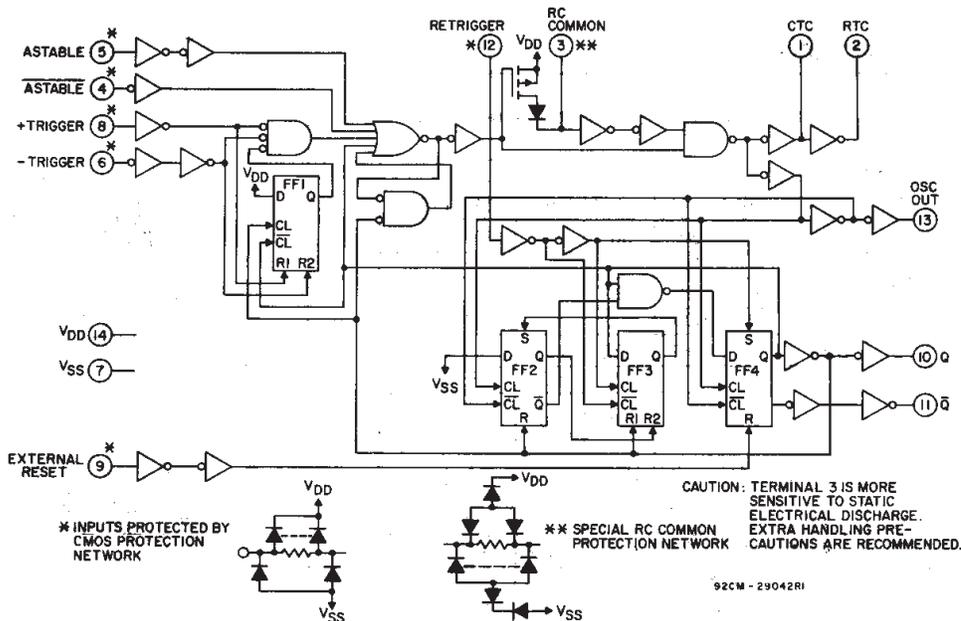


Fig. 2—CD4047B logic diagram.

92CM-29042R1