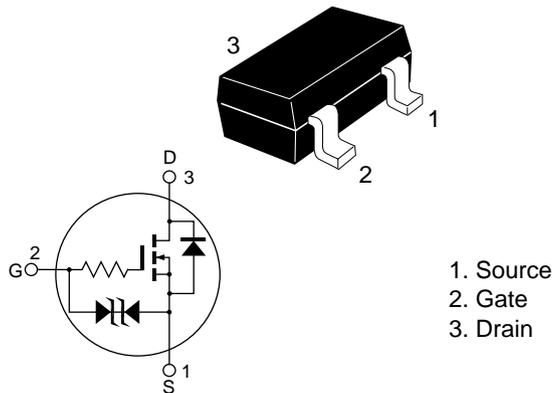# 2SK3000

Silicon N Channel MOS FET
Low Frequency Power Switching

HITACHI

Features

- Low on-resistance
  $R_{DS(on)} = 0.25\Omega$ typ. ($V_{GS} = 10$ V, $I_D = 450$ mA)
- 4V gate drive devices.
- Small package (MPAK)
- Expansive drain to source surge power capability

Outline

MPAK

1. Source
2. Gate
3. Drain

2SK3000

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	1.0	A
Drain peak current	$I_{D(pulse)}$ Note1	4.0	A
Reverse drain current	I_{DR}	1.0	A
Channel dissipation	Pch Note2	400	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. When using the glass epoxy board (10 mm x 10 mm x 1 mm^t)

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	60	V	I_D = 100μA, V_{GS} = 0
Drain to source voltage	$V_{DS(SUS)}$	40	—	—	V	L = 100μH, I_D = 3 A
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±100μA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	1.0	μA	V_{DS} = 40 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	μA	V_{GS} = ±6.5V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.1	—	2.1	V	I_D = 10μA, V_{DS} = 5V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.5	Ω	I_D = 450 mA V_{GS} = 4V Note3
Static drain to source on state resistance	$R_{DS(on)}$	—	0.25	0.3	Ω	I_D = 450 mA V_{GS} = 10V Note3
Forward transfer admittance	$|y_{fs}|$	0.5	1.2	—	S	I_D = 450 mA V_{DS} = 10V Note3
Input capacitance	Ciss	—	14.0	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	68	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	3.0	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	0.12	—	μs	V_{GS} = 4V, I_D = 450 mA
Rise time	t_r	—	0.6	—	μs	R_L = 22Ω
Turn-off delay time	$t_{d(off)}$	—	1.7	—	μs	
Fall time	t_f	—	1.4	—	μs	

Note: 3. Pulse test
4. Marking is "ZY".