



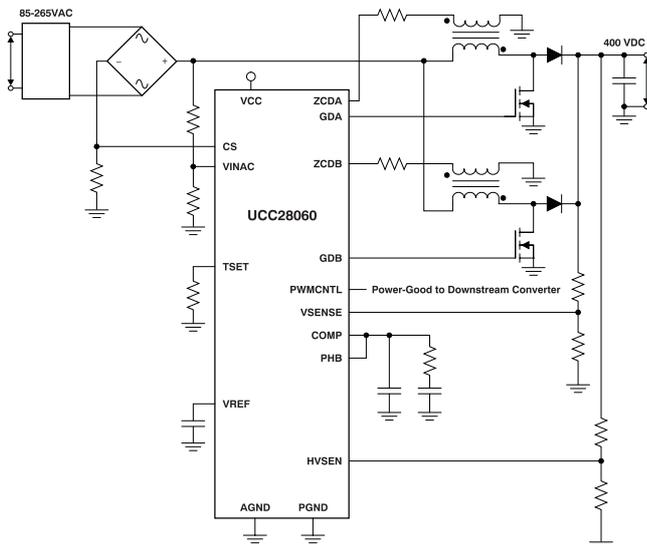
Natural Interleaving™ DUAL-PHASE TRANSITION-MODE PFC CONTROLLER

NATURAL INTERLEAVING FEATURES

- Easy Phase Management Facilitates Compliance to Light-Load Efficient Standards
- FailSafe OVP with Dual Paths Prevents Output Over-voltage Conditions Caused by Voltage-Sensing Failures
- Sensorless Current Shaping Simplifies Board Layout and Improves Efficiency
- Inrush Safe Current Limiting:
 - Prevents MOSFET conduction during inrush
 - Eliminates reverse recovery events in output rectifiers

SYSTEM FEATURES

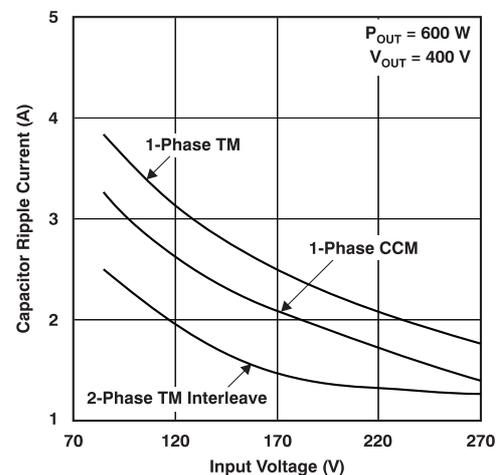
- Cost Savings
- Improved Efficiency and Design Flexibility over Traditional, Single-Phase Continuous Conduction Mode (CCM)
- Input Filter and Output Capacitor Current Cancellation:
 - Reduced current ripple for higher system reliability and smaller bulk capacitor
 - Reduced EMI filter size
- Enables Use of Low-Cost Diodes without Extensive Snubber Circuitry
- Improved Light-Load Efficiency
- Improved Transient Response
- Complete System-Level Protection
- 1-A Source/1.8-A Sink Gate Drivers
- Operating Temperature Range: -40°C to $+125^{\circ}\text{C}$ in an SOIC 16-pin package



Typical Application Circuit

APPLICATIONS

- 100-W to 800-W Power Supplies
- LCD, Plasma, and DLP® TVs
- Computer Power Supplies
- Entry Level Servers
- Electronic Lighting Ballasts



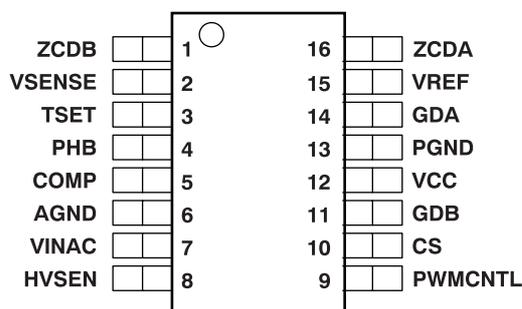
Ripple Current Reduction



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DEVICE INFORMATION
**UCC28060D
SOIC 16-Pin (D)
Top View**

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
AGND	6	—	Analog ground: Connect analog signal bypass capacitors, compensation components, and analog signal returns to this pin. Connect the analog and power grounds at a single point to isolate high-current noise signals of the power components from interference with the low-current analog circuits.
COMP	5	O	Error amplifier output: The error amplifier is a transconductance amplifier, so this output is a high-impedance current source. Connect voltage regulation loop compensation components from this pin to AGND. The on-time seen at the gate drive outputs is proportional to the voltage at this pin minus an offset of approximately 125 mV. During soft-start events (undervoltage, brownout, or disable), COMP is pulled low. Normal operation only resumes after the soft-start event clears and COMP has been discharged below 0.5 V, making sure that the circuit restarts with a low COMP voltage and a short on-time. Do not connect COMP to a low-impedance source that would interfere with COMP falling below 0.5 V.
CS	10	I	Current sense input: Connect the current sense resistor and the negative terminal of the diode bridge to this pin. Connect the return of the current sense resistor to the AGND pin with a separate trace. As input current increases, the voltage on CS goes more negative. This cycle-by-cycle over-current protection limits input current by turning off both gate driver (GDx) outputs when CS is more negative than the CS rising threshold (approximately –200 mV). The GD outputs remain low until CS falls to the CS falling threshold (approximately –15 mV). Current sense is blanked for approximately 100 ns following the falling edge of either GD output. This blanking filters noise that occurs when current switches from a power FET to a boost diode. In most cases, no additional current sense filtering is required. If filtering is required, the filter series resistance must be under 100 Ω to maintain accuracy. To prevent excessive negative voltage on the CS pin during inrush conditions, connect the current sensing resistor to the CS pin through a low value external resistor. As with the filter series resistance, this external resistor needs to be under 100 Ω to maintain accuracy.
GDA	14	O	Channel A and channel B gate drive output: Connect these pins to the gate of the power FET for each phase through the shortest connection practical. If it is necessary to use a trace longer than 0.5 in (12.6 mm) for this connection, some ringing may occur due to trace series inductance. This ringing can be reduced by adding a 5-Ω to 10-Ω resistor in series with GDA and GDB.
GDB	11	O	
HVSEN	8	I	High voltage output sense: The UCC28060 incorporates FailSafe OVP so that any single failure does not allow the output to boost above safe levels. Output over-voltage is monitored by both VSENSE and HVSEN and shuts down the PWM if either pin exceeds the appropriate over-voltage threshold. Using two pins to monitor for over-voltage provides redundant protection and fault tolerance. HVSEN can also be used to enable a downstream power converter when the voltage on HVSEN is within the operating region. Select the HVSEN divider ratio for the desired over-voltage and power-good thresholds. Select the HVSEN divider impedance for the desired power-good hysteresis. During operation, HVSEN must never fall below 0.8 V. Dropping HVSEN below 0.8 V puts the UCC28060 into a special test mode, used only for factory testing. A bypass capacitor from HVSEN to AGND is recommended to filter noise and prevent false over-voltage shutdown.
PGND	13	—	Power ground for the integrated circuit: Connect this pin to AGND through a separate short trace to isolate gate driver noise from analog signals.

TERMINAL FUNCTIONS (continued)

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
PHB	4	I	Phase B enable: This pin turns on/off channel B of the boost converter. The commanded on-time for channel A is immediately doubled when channel B is disabled, which helps to keep COMP voltage constant during the phase management transient. The PHB thresholds change with line range for the best efficiency when PHB is connected to COMP. PHB can also be driven by external logic signals to allow customized phase management. To disable phase management, connect the PHB pin to the VREF pin.
PWMCNTL	9	O	PWM enable logic output: This open-drain output goes low when HVSEN is within the HVSEN good region and the ZCDA and ZCDB inputs are switching correctly if operating in two-phase mode (see PHB Pin). Otherwise, PWMCNTL is high impedance.
TSET	3	I	Timing set: PWM on-time programming input. Connect a resistor from TSET to AGND to set the on-time versus COMP voltage and the minimum period at the gate drive outputs.
VCC	12	—	Bias supply input: Connect this pin to a controlled bias supply of between 14 V and 21 V. Also connect a 0.1- μ F ceramic bypass capacitor from this pin to PGND. This supply powers all circuits in the device and must be capable of delivering 6 mA dc plus the transient power MOSFET gate charging current.
VINAC	7	I	Input ac voltage sense: For normal operation, connect this pin to a voltage divider across the rectified input power mains. This input senses input voltage range to set the ramp rate and senses brownout. Input voltage range changes when the peak voltage on VINAC becomes and stays below the range change threshold for the range change filter time or the peak voltage on VINAC becomes above the range change threshold. When the voltage on VINAC remains below the brownout threshold for more than the brownout filter time, the device enters a brownout mode and both output drives are disabled. Select the input voltage divider ratio for the desired brownout threshold and power line range. Select the divider impedance for the desired brownout hysteresis.
VREF	15	O	Voltage reference output: Connect a 0.1- μ F ceramic bypass capacitor from this pin to AGND. This 6 VDC reference can be used to bias other circuits requiring less than 2 mA of total supply current.
VSENSE	2	I	Output dc voltage sense: Connect this pin to a voltage divider across the output of the power converter. The error amplifier reference voltage is 6 V. Select the output voltage divider ratio for the desired output voltage. Connect the ground side of this divider to ground through a separate short trace for best output regulation accuracy and noise immunity. VSENSE can be pulled low by an open-drain logic output or 6-V logic output in series with a low-leakage diode to disable the outputs and reduce VCC current. If VSENSE is disconnected, open-loop protection provides an internal current source to pull VSENSE low, turning off the gate drivers.
ZCDA	16	I	Zero current detection inputs: These inputs expect to see a negative edge when the inductor current in the respective phases go to zero. The inputs are clamped at 0 V and 3 V. Signals should be coupled through a series resistor that limits the clamping current to less than ± 3 mA. Connect these pins through a current limiting resistor to the zero crossing detection windings of the appropriate boost inductor. The inductor winding must be connected so that this voltage drops when inductor current decays to zero. When the inductor current drops to zero, the ZCD input must drop below the falling threshold, approximately 1 V, to cause the gate drive output to rise. When the power MOSFET turns off, the ZCD input must rise above the rising threshold, approximately 1.7 V, to arm the logic for another falling ZCD edge.
ZCDB	1	I	

FUNCTIONAL BLOCK DIAGRAM

