BIAS POWER SUPPLY FOR TV AND MONITOR TFT LCD PANELS

FEATURES

- 8-V to 14-V Input Voltage Range
- V_S Output Voltage Range up to 19 V
- 1% Accurate Boost Converter With 2.8-A Switch Current
- 1.5% accurate 2.3-A Step-Down Converter
- 500-kHz/750-kHz Fixed Switching Frequency
- Negative Charge Pump Driver for VGL
- Positive Charge Pump Driver for VGH
- Adjustable Sequencing for VGL, VGH
- Gate Drive Signal to Drive External MOSFET
- Internal and Adjustable Soft Start
- Short-Circuit Protection
- Overvoltage Protection
- Thermal Shutdown
- Available in TSSOP-28 Package

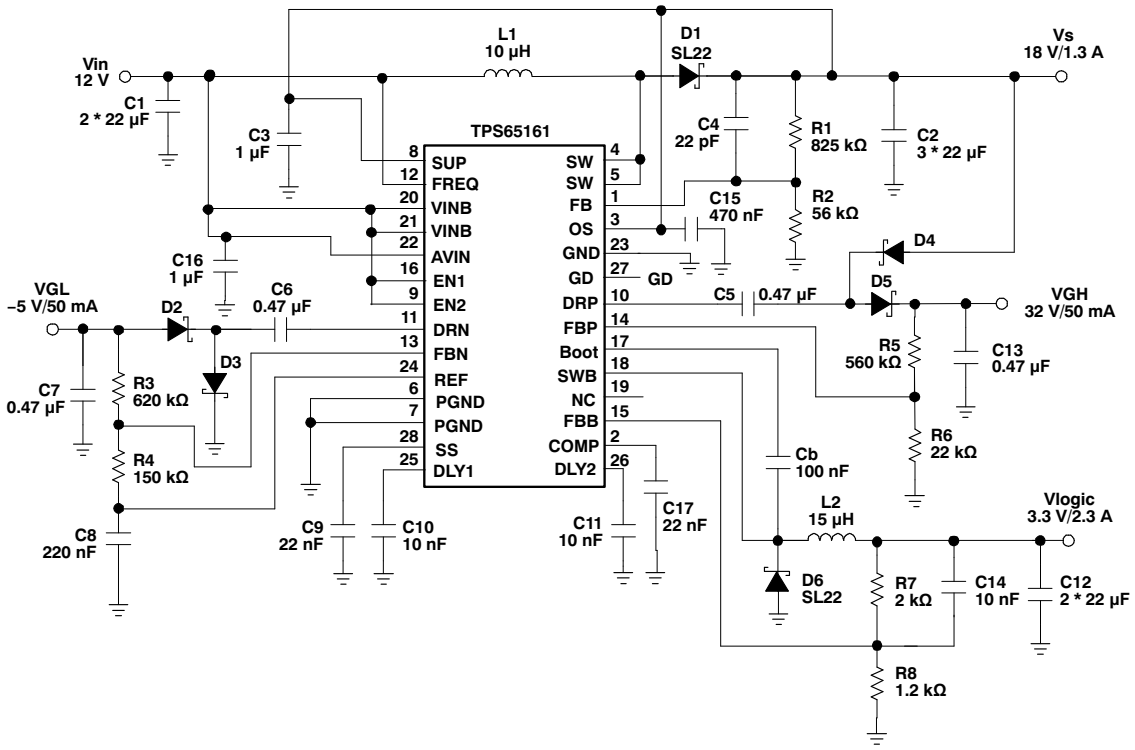
APPLICATIONS

- TFT LCD Displays for Monitor and LCD TV

DESCRIPTION

The TPS65161 offers a compact power supply solution to provide all four voltages required by thin-film transistor (TFT) LCD panel. With its high current capabilities, the device is ideal for large screen monitor panels and LCD TV applications.

TYPICAL APPLICATION

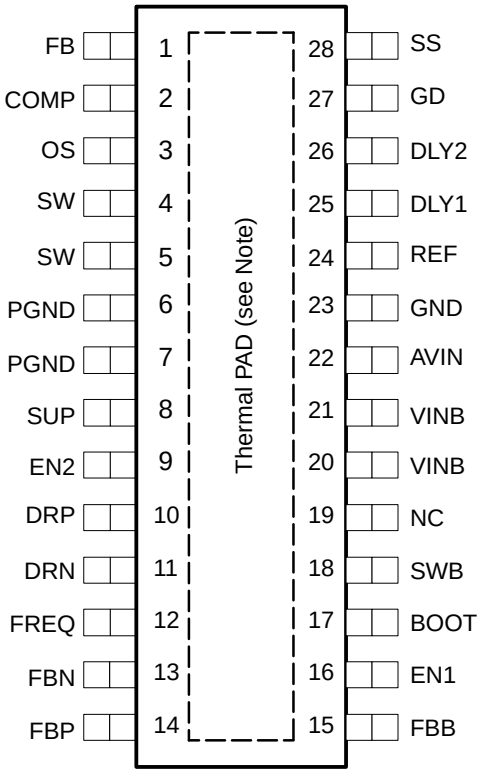


ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, SUP = V_{IN}, EN1 = EN2 = V_{IN}, V_S = 15 V, V_{LOGIC} = 3.3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NEGATIVE CHARGE-PUMP VGL						
VGL	Output voltage range				–2	V
V_{FBN}	Feedback regulation voltage		–36	0	36	mV
I_{FBN}	Feedback input bias current			10	100	nA
$r_{DS(ON)}$	Q4 P-Channel switch $r_{DS(ON)}$	I_{OUT} = 20 mA		4.4		Ω
V_{DropN}	Current sink voltage drop (10)	I_{DRN} = 50 mA, V_{FBN} = $V_{FBNnominal}$ –5%		130	190	mV
		I_{DRN} = 100 mA, V_{FBN} = $V_{FBNnominal}$ –5%		270	420	
POSITIVE CHARGE-PUMP OUTPUT VGH						
V_{FBP}	Feedback regulation voltage		1.187	1.213	1.238	V
I_{FBP}	Feedback input bias current			10	100	nA
$r_{DS(ON)}$	Q3 N-Channel switch $r_{DS(ON)}$	I_{OUT} = 20 mA		1.1		Ω
V_{DropP}	Current source voltage drop (Vsup – V_{DRP}) (3)	I_{DRP} = 50 mA, V_{FBP} = $V_{FBPnominal}$ –5%		400	680	mV
		I_{DRP} = 100 mA, V_{FBP} = $V_{FBPnominal}$ –5%		850	1600	

(10) The maximum charge-pump output current is typically half the drive current of the internal current source or current sink.



NOTE: The thermally enhanced PowerPAD™ is connected to PGND.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SUP	8	I	This is the supply pin of the positive charge pump driver and can be connected to the input supply Vin or the output of the main boost converter Vs. This depends mainly on the desired output voltage VGH and numbers of charge pump stages.
FREQ	12	I	Frequency adjust pin. This pin allows setting the switching frequency with a logic level to 500 kHz = low and 750 kHz = high.
AVIN	22	I	Analog input voltage of the device. This is the input for the analog circuits of the device and should be bypassed with a 1-µF ceramic capacitor for good filtering.
VINB	20, 21	I	Power input voltage pin for the buck converter.
EN1	16	I	This is the enable pin of the buck converter and negative charge pump. When this pin is pulled high, the buck converter starts up, and after a delay time set by DLY1, the negative charge pump comes up. This pin must be terminated and not be left floating. A logic high enables the device and a logic low shuts down the device.
EN2	9	I	The boost converter starts only with EN1 = high, after the step-down converter is enabled. EN2 is the enable pin of the boost converter and positive charge pump. When this pin is pulled high, the boost converter and positive charge pump starts up after the buck converter is within regulation and a delay time set by DLY2 has passed by. This pin must be terminated and not be left floating. A logic high enables the device and a logic low shuts down the device.
DRN	11	O	Drive pin of the negative charge pump.
FBN	13	I	Feedback pin of negative charge pump.
REF	24	O	Internal reference output typically 1.213 V
PGND	6, 7		Power ground
SS	28	O	This pin allows setting the soft-start time for the main boost converter V_S. Typically a 22-nF capacitor needs to be connected to this pin to set the soft-start time.
DLY1	25	O	Connecting a capacitor from this pin to GND allows the setting of the delay time between V_{LOGIC} (step-down converter output high) to VGL during start-up.
DLY2	26	O	Connecting a capacitor from this pin to GND allows the setting of the delay time between V_{LOGIC} (step-down converter output high) to V_S Boost converter and positive charge-pump VGH during start-up.
COMP	2		This is the compensation pin for the main boost converter. A small capacitor and, if required, a resistor is connected to this pin.
FBB	15	I	Feedback pin of the buck converter
SWB	18	O	Switch pin of the buck converter
NC	19		Not connected
BOOT	17	I	N-channel MOSFET gate drive voltage for the buck converter. Connect a capacitor from the switch node SWB to this pin.
FBP	14	I	Feedback pin of positive charge pump.
DRP	10	O	Drive pin of the positive charge pump.
GD	27		This is the gate drive pin which can be used to control an external MOSFET switch to provide input to output isolation of V_S or VGH. See the circuit diagrams at the end of this data sheet. GD is an open-drain output and is latched low as soon as the boost converter is within 8% of its nominal regulated output voltage. GD goes high impedance when the EN2 input voltage is cycled low.
GND	23		Analog ground
OS	3	I	Output sense pin. The OS pin is connected to the internal rectifier switch and overvoltage protection comparator. This pin needs to be connected to the output of the boost converter and cannot be connected to any other voltage rail. Connect a 470-nF capacitor from OS pin to GND to avoid noise coupling into this pin. The PCB trace of the OS pin needs to be wide because it conducts high current.
FB	1	I	Feedback of the main boost converter generating Vsource (V_S).
SW	4, 5	I	Switch pin of the boost converter generating Vsource (V_S).
PowerPAD			The PowerPAD needs to be connected and soldered to power ground (PGND).

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
MAIN BOOST CONVERTER (Vs)			
η	Efficiency main boost converter Vs	vs Load current V_S =15 V,V_{IN} = 12 V	1
$r_{DS(ON)}$	N-channel main switch Q1	vs Input voltage and temperature	2
	Soft-start boost converter	C_{SS} = 22 nF	3
	PWM operation at full-load current		4
	PWM operation at light-load current		5
	Load transient response		6
STEP-DOWN CONVERTER (Vlogic)			
η	Efficiency main boost converter V_S	vs Load current V_{LOGIC} = 3.3 V,V_{IN} = 12 V	7
$r_{DS(ON)}$	N-channel main switch Q1		8
	PWM operation - continuous mode		9
	PWM operation - discontinuous mode		10
	Soft start		11
	Load transient response		12
SYSTEM PERFORMANCE			
f_{osc}	Oscillation frequency	vs Input voltage and temperature	13
	Power-up sequencing	EN2 connected to V_{IN}	14
	Power-up sequencing	EN2 enabled separately	15

BOOST CONVERTER EFFICIENCY vs OUTPUT CURRENT

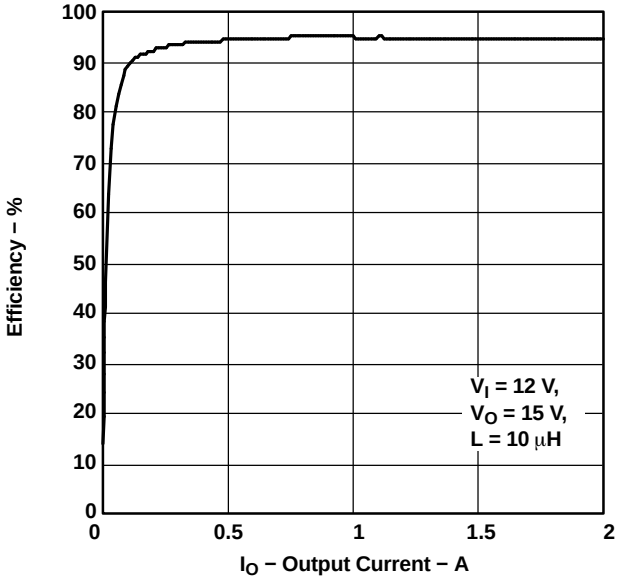


Figure 1.

BOOST CONVERTER $r_{DS(ON)}$ - N-CHANNEL SWITCH vs TEMPERATURE

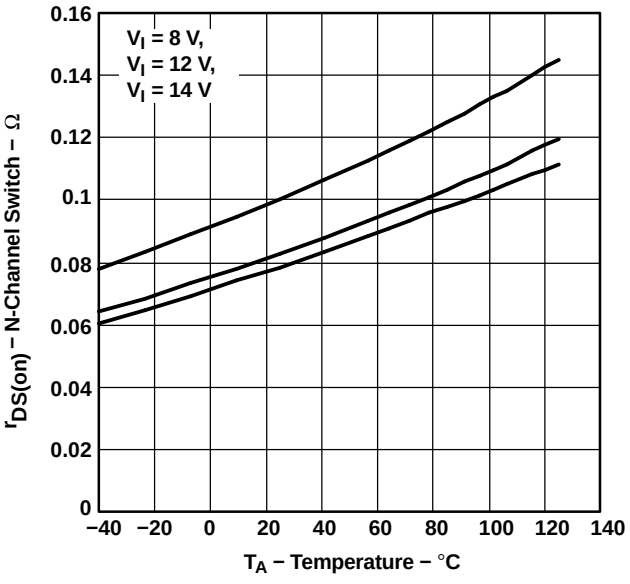


Figure 2.