FAIRCHILD SEMICONDUCTOR TM

March 1999

FDV301N
Digital FET , N-Channel

General Description

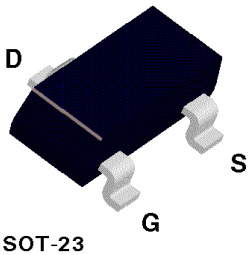
This N-Channel logic level enhancement mode field effect transistor is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, this one N-channel FET can replace several different digital transistors, with different bias resistor values.

Features

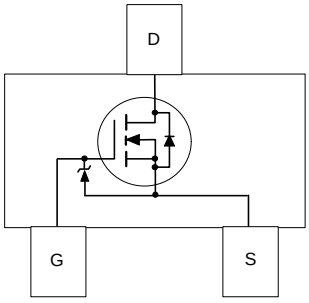
- 25 V, 0.22 A continuous, 0.5 A Peak.
  $R_{DS(ON)}$ = 5 Ω @ V_{GS}= 2.7 V
  $R_{DS(ON)}$ = 4 Ω @ V_{GS}= 4.5 V.
- Very low level gate drive requirements allowing direct operation in 3V circuits. $V_{GS(th)}$ < 1.5V.
- Gate-Source Zener for ESD ruggedness. >6kV Human Body Model
- Replace multiple NPN digital transistors with one DMOS FET.

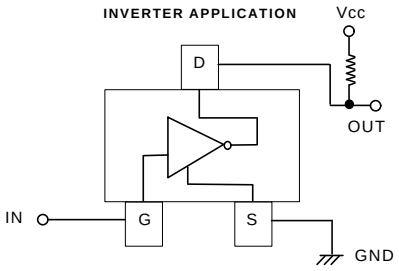
SOT-23 | **SuperSOT™-6** | **SuperSOT™-8** | **SO-8** | **SOT-223** | **SOIC-16**

Mark:301



SOT-23





Absolute Maximum Ratings T_A = 25°C unless other wise noted

Symbol	Parameter	FDV301N	Units
V_{DSS}, V_{CC}	Drain-Source Voltage, Power Supply Voltage	25	V
V_{GSS}, V_I	Gate-Source Voltage, V_{IN}	8	V
I_D, I_O	Drain/Output Current - Continuous	0.22	A
		0.5	
P_D	Maximum Power Dissipation	0.35	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6.0	kV
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	357	°C/W