CD4094B Types

CMOS
8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

■ CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

■ 3-state parallel outputs for connection to common bus
■ Separate serial outputs synchronous to both positive and negative clock edges for cascading
■ Medium speed operation -- 5 MHz at 10 V (typ.)
■ Standardized, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package temperature range):
  1 V at V_{DD} = 5 V   2 V at V_{DD} = 10 V
              2.5 V at V_{DD} = 15 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

■ Serial-to-parallel data conversion
■ Remote control holding register
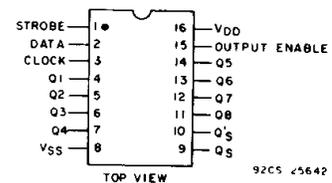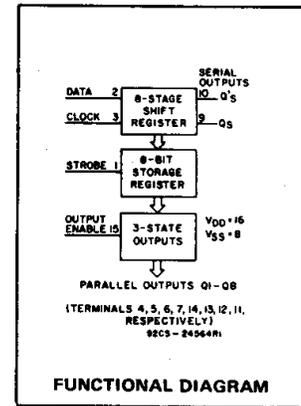■ Dual-rank shift, hold, and bus applications

FUNCTIONAL DIAGRAM

Fig. 1 – Terminal assignment.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal) .... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = −55°C to +100°C 500mW
  For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
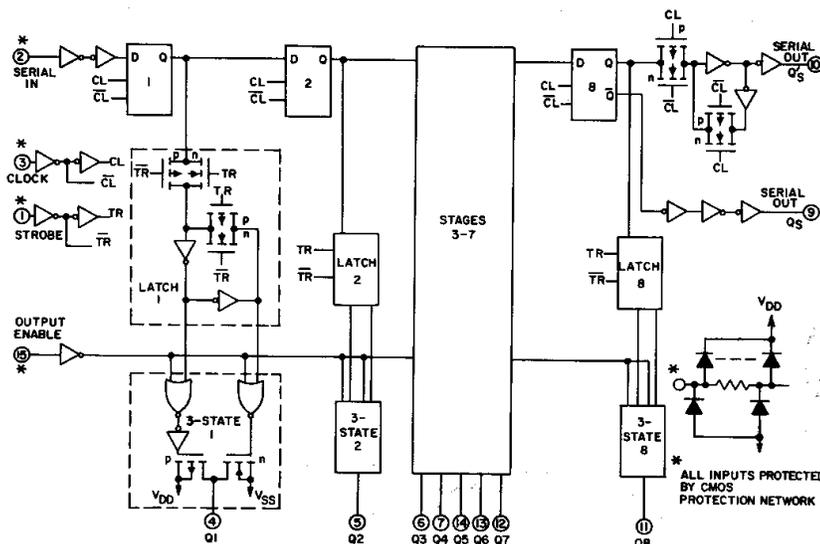 At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

Fig. 2 – CD4094B Logic diagram.

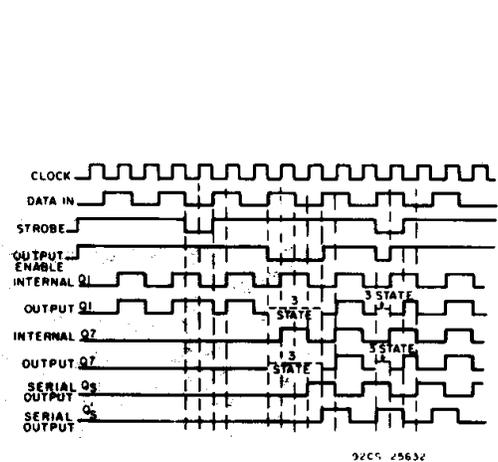*Fig. 3 – Timing diagram.*

CD4094B Types

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that
operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	125	–	ns
	10	55	–	
	15	35	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	83	–	
Clock Input Frequency, f_{CL}	5	dc	1.25	MHz
	10		2.5	
	15		3	
Clock Input Rise or Fall time, t_rCL, t_fCL:*	5	–	15	μs
	10		5	
	15		5	
Strobe Pulse Width, t_W	5	200	–	ns
	10	80	–	
	15	70	–	

*If more than one unit is cascaded t_fCL (for Q_S only) should be made less than or equal
to the sum of the fixed propagation delay at 50 pF and the transition time of the output
driving stage for the estimated capacitive load.

TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
⌐/	0	X	X	OC	OC	Q7	NC
_/	0	X	X	OC	OC	NC	Q7
_/	1	0	X	NC	NC	Q7	NC
_/	1	1	0	0	Q_{N-1}	Q7	NC
⌐\	1	1	1	1	Q_{N-1}	Q7	NC
	1	1	1	NC	NC	NC	Q7

▲ = Level Change   Logic 1 ≡ High
X = Don't Care   Logic 0 ≡ Low
NC = No Change
OC = Open Circuit

* At the positive clock edge information in the 7th shift register
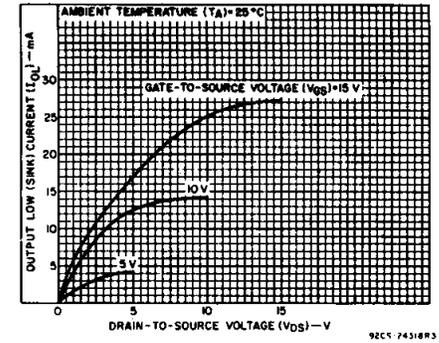stage is transferred to the 8th register stage and the Q_S output.

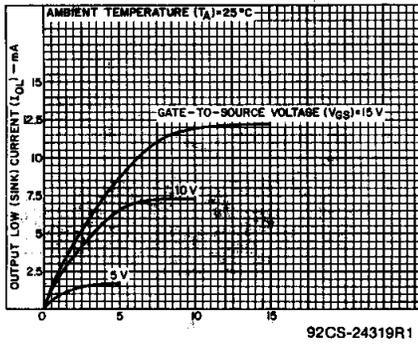Fig. 4 — Typical output low (sink) current characteristics.

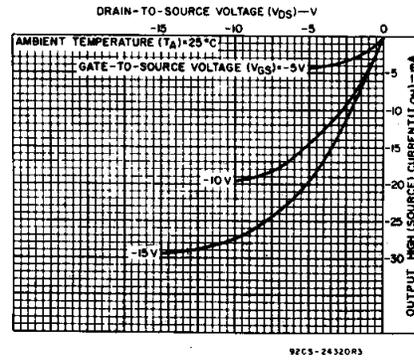Fig. 5 — Minimum output low (sink) current characteristics.

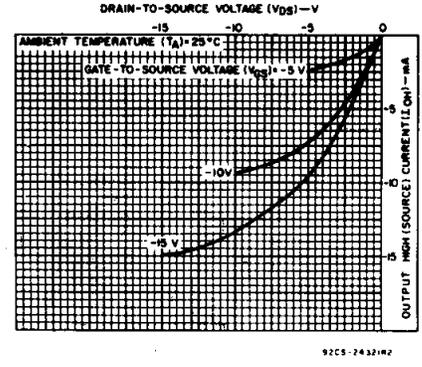Fig. 6 — Typical output high (source) current characteristics.

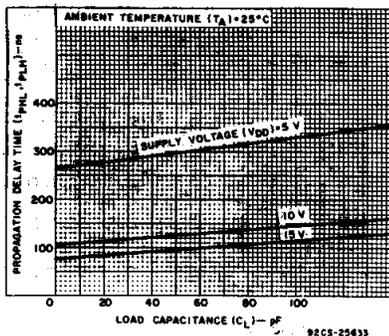Fig. 7 — Minimum output high (source) current characteristics.

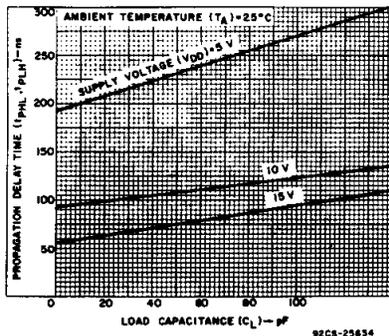Fig. 8 — Clock-to-serial output Q_S propagation delay vs C_L.

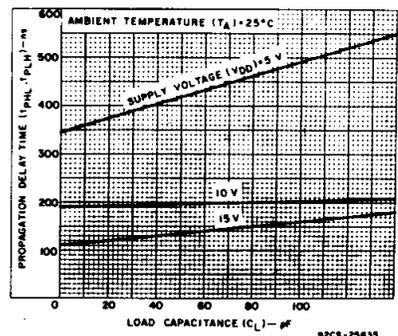Fig. 9 — Clock-to-serial output Q'_S propagation delay vs C_L.

Fig. 10 — Clock-to-parallel output propagation delay vs C_L.

COMMERCIAL CMOS
HIGH VOLTAGE ICs

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