

MOS FIELD EFFECT TRANSISTOR 2SK4075

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4075 is N-channel MOS FET designed for high current switching applications.

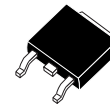
ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4075-ZK-E1-AY	Pure Sn (Tin)	Tape	TO-252 (MP-3ZK)
2SK4075-ZK-E2-AY		2500 p/reel	typ. 0.27 g

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 6.7 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 30 \text{ A)}$
 $R_{DS(on)2} = 10 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 15 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2900 \text{ pF TYP.}$
- Logic level drive type

(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	40	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±60	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±180	A
Total Power Dissipation (T _C = 25°C)	P _{T1}	52	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current ^{Note2}	I _{AS}	28	A
Single Avalanche Energy ^{Note2}	E _{AS}	78	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 20 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

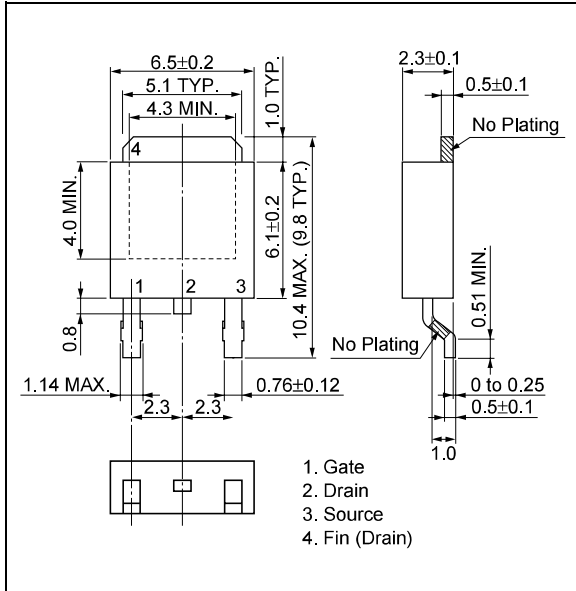
THERMAL RESISTANCE

Channel to Case Thermal Resistance	R _{th(ch-C)}	2.4	°C/W
Channel to Ambient Thermal Resistance	R _{th(ch-A)}	125	°C/W

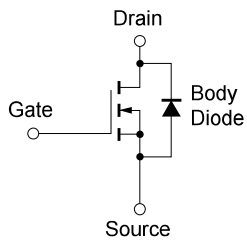
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PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.