

CD4017B, CD4022B Types

CMOS Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4017B—Decade Counter with
10 Decoded Outputs

CD4022B—Octal Counter with
8 Decoded Outputs

■ CD4017B and CD4022B are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high-speed operation, 2-input decode-gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the CD4017B or every 8 clock input cycles in the CD4022B and is used to ripple-clock the succeeding device in a multi-device counting chain.

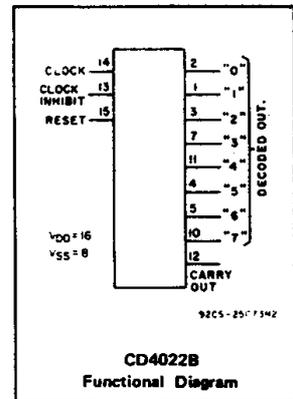
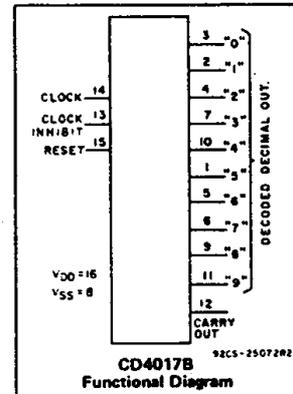
Features:

- Fully static operation
- Medium-speed operation . . . 10 MHz (typ.) at $V_{DD} = 10\text{ V}$
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Decade counter/decimal decode display (CD4017B)
- Binary counter/decoder
- Frequency division
- Counter control/timers
- Divide-by-N counting
- For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"

The CD4017B and CD4022B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic package (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4017B types also are supplied in 16-lead small-outline packages (M and M96 suffixes).



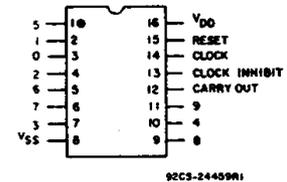
3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

RECOMMENDED OPERATING CONDITIONS

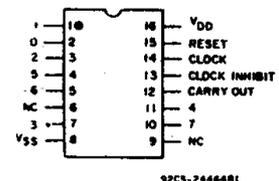
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Clock Input Frequency, f_{CL}	5	—	2.5	MHz
	10	—	5	
	15	—	5.5	
Clock Pulse Width, t_W	5	200	—	ns
	10	90	—	
	15	60	—	
Clock Rise & Fall Time, t_{rCL} , t_{fCL}	5	UNLIMITED*		
	10	UNLIMITED*		
	15	UNLIMITED*		
Clock Inhibit Setup Time, t_s	5	230	—	ns
	10	100	—	
	15	70	—	
Reset Pulse Width, t_{RW}	5	260	—	ns
	10	110	—	
	15	60	—	
Reset Removal Time, t_{rem}	5	400	—	ns
	10	280	—	
	15	150	—	

*Only if Pin 14 is used as the clock input. If Pin 13 is used as the clock input and Pin 14 is tied high (for advancing count on negative transition of the clock), rise and fall time should be $\leq 15\ \mu\text{s}$.



TOP VIEW
CD4017B
TERMINAL DIAGRAM



TOP VIEW
NC - no connection
CD4022B
TERMINAL DIAGRAM

CD4017B, CD4022B Types

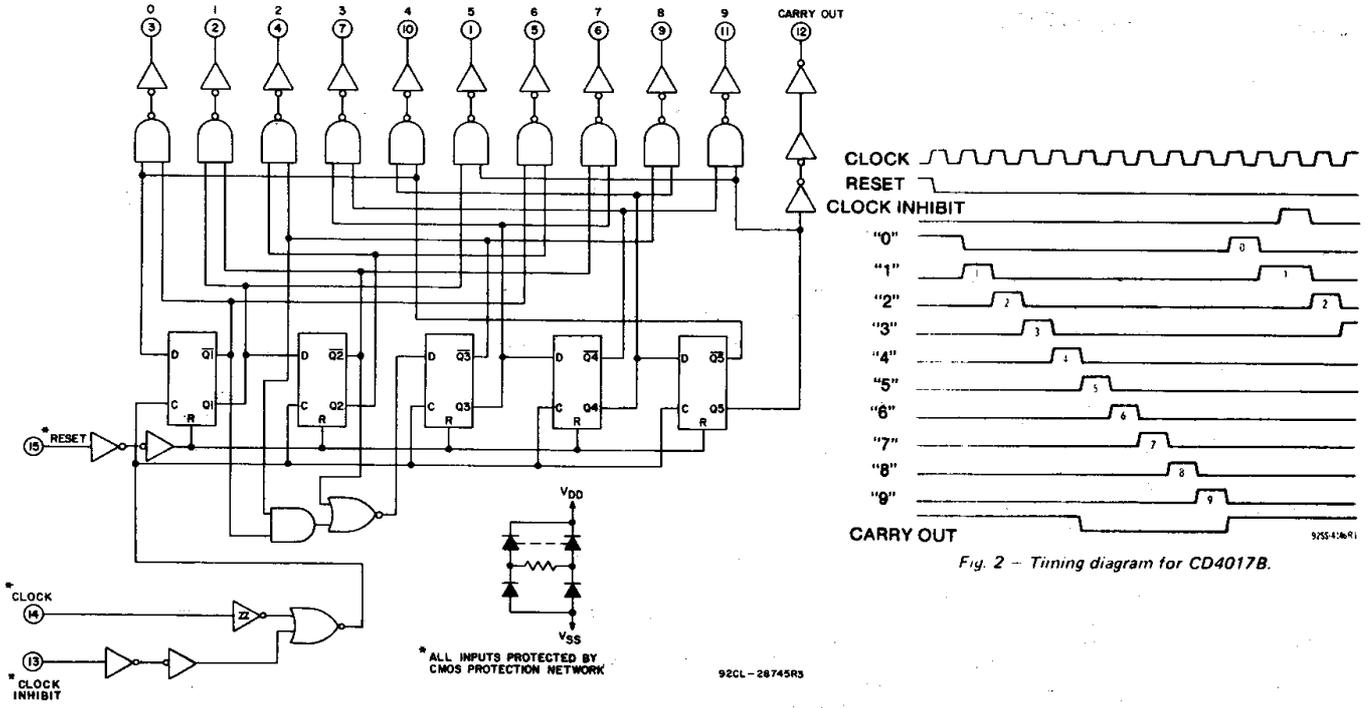


Fig. 2 - Timing diagram for CD4017B.

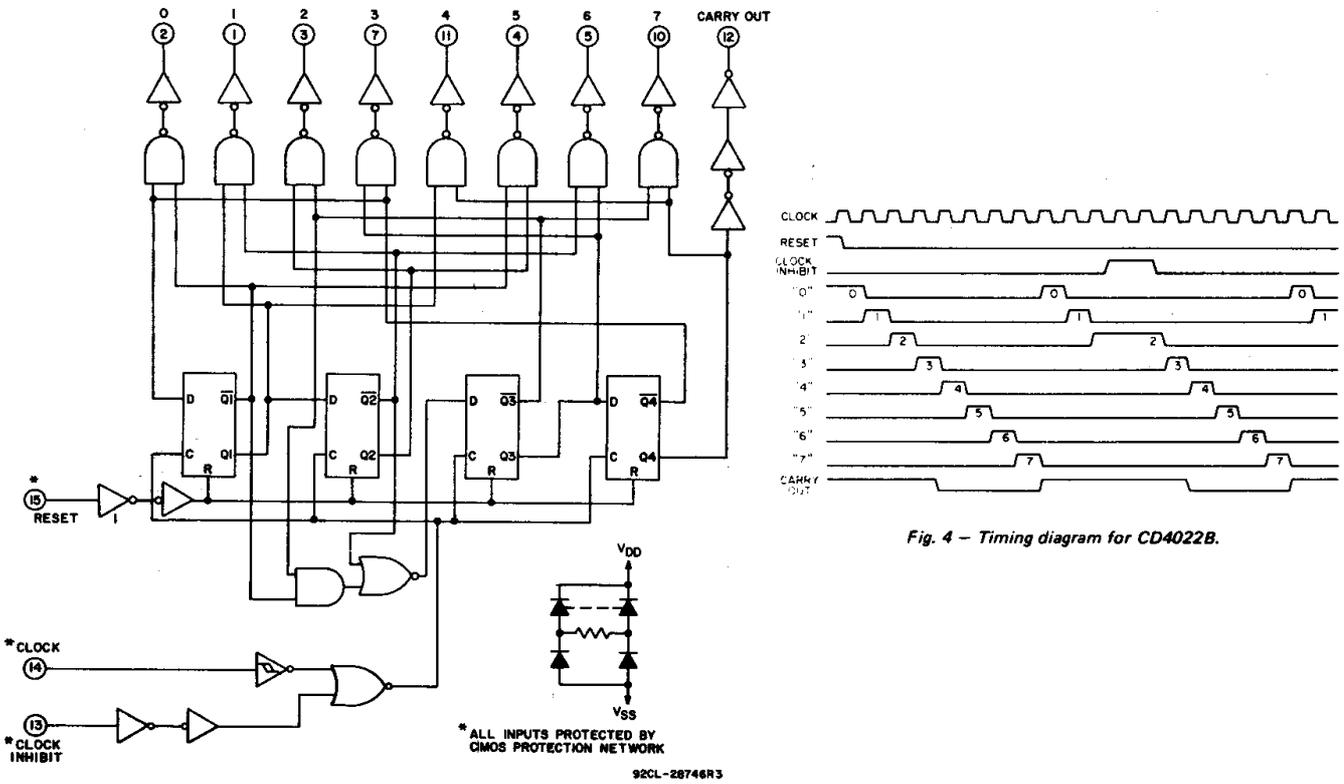


Fig. 4 - Timing diagram for CD4022B.

Fig. 3 - Logic diagram for CD4022B.