

TLP155E

Plasma Display Panel (PDP)
Industrial Inverter
MOS FET / IGBT Gate Driver

Unit: mm

The Toshiba TLP155E consists of an infrared emitting diodes and integrated high gain, high-speed photodetectors. The TLP155E is housed in the SO6 package.

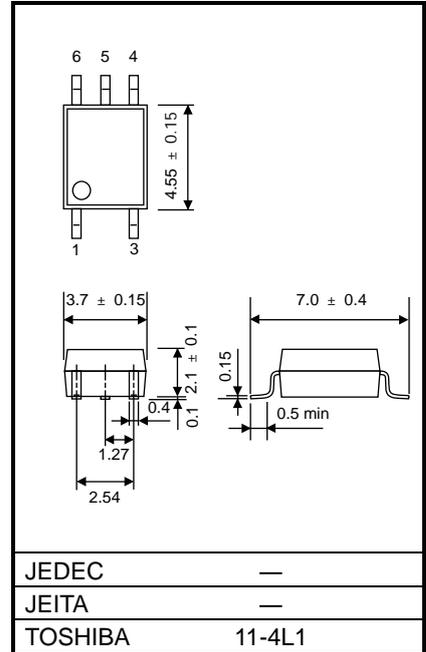
The photodetector has an internal Faraday shield that provides a guaranteed common-mode transient immunity of ± 15 kV/ μ s. TLP155E is suitable for direct gate driving circuit for IGBTs or power MOSFETs.

- Buffer logic type (Totem pole output)
- Package type: SO6
- Peak Output Current : $I_{OP} = \pm 0.6$ A (max)
- Guaranteed performance over temperature: -40 to 100 °C
- Threshold Input Current: $I_{FLH} = 7.5$ mA (max)
- Propagation delay time : $t_{pLH} / t_{pHL} = 200$ ns (max)
- Common mode transient immunity : ± 15 kV/ μ s (min)
- Isolation voltage : 3750 V_{rms} (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
File No.E67349
- VDE-approved: EN 60747-5-5, EN 62368-1 (Note 1)
- CQC-approved: GB4943.1, GB8898 Thailand Factory



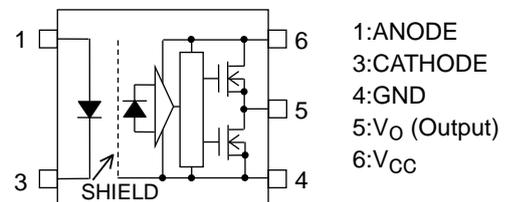
仅适用于海拔 2000m 以下地区安全使用

Note 1: When a EN 60747-5-5 approved type is needed, please designate the **Option(V4)**.



weight: 0.08 g (typ.)

Pin Configuration (Top View)



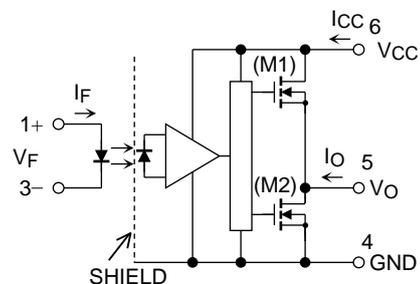
Truth Table

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

Construction Mechanical Ratings

Creepage distance	5.0 mm (min)
Clearance distance	5.0 mm (min)
Insulation thickness	0.4 mm (min)

Schematic



Start of commercial production
2010-08

Absolute Maximum Ratings (Ta = 25 °C)

Characteristics		Symbol	Rating	Unit
LED	Forward Current	I_F	20	mA
	Forward Current Derating (Ta ≥ 92°C)	$\Delta I_F / ^\circ\text{C}$	-0.63	mA/°C
	Pulse Forward Current (Note 1)	I_{FPT}	1	A
	Reverse Voltage	V_R	5	V
	Input Power Dissipation	PD	40	mW
	Input Power Dissipation Derating (Ta ≥ 92°C)	$\Delta PD / ^\circ\text{C}$	-1.2	mW/°C
	Junction Temperature	T_j	125	°C
DETECTOR	"H" Peak Output Current (Note 2)	I_{OPH}	-0.6	A
	"L" Peak Output Current (Note 2)	I_{OPL}	0.6	A
	Output Voltage	V_O	35	V
	Supply Voltage	V_{CC}	35	V
	Output Power Dissipation	PO	80	mW
	Output Power Dissipation Derating (Ta ≥ 85°C)	$\Delta PO / ^\circ\text{C}$	-2.0	mW/°C
	Junction Temperature	T_j	125	°C
Operating frequency (Note 3)		f	250	kHz
Operating Temperature Range		T_{opr}	-40 to 100	°C
Storage Temperature Range		T_{stg}	-55 to 125	°C
Lead Soldering Temperature (10 s)		T_{sol}	260	°C
Isolation Voltage (AC, 60 s, R.H. ≤ 60 %) (Note 4)		BV_S	3750	V_{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width ≤ 1 μs, 300 pps.

Note 2: Exponential waveform pulse width $P_W \leq 2 \mu\text{s}$, $f \leq 10 \text{ kHz}$, $V_{CC} = 20 \text{ V}$, $T_a = -40 \text{ to } 100 \text{ }^\circ\text{C}$

Note 3: Exponential waveform pulse width $P_W \leq 80 \text{ ns}$, $I_{OPH} \geq -0.25 \text{ A}$, $I_{OPL} \leq 0.25 \text{ A}$, $V_{CC} = 20\text{V}$, $T_a = -40 \text{ to } 100 \text{ }^\circ\text{C}$

Note 4: This device is regarded as a two terminal device: pins 1 and 3 are shorted together, as are pins 4, 5 and 6.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input Current, High Level (Note 1)	I_{FLH}	10	-	15	mA
Input Voltage, Low Level	V_{FHL}	0	-	0.8	V
Supply Voltage*	V_{CC}	10	-	30	V
Peak output current	I_{OPH}/ I_{OPL}	-	-	±0.2	A
Operating Temperature	T_{opr}	-40	-	100	°C

* This item denotes operating range, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: Input signal rise time (fall time) < 0.5 μs.

Electrical Characteristics (Ta = -40 to 100 °C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit	
Forward voltage		V _F	—	I _F = 10 mA, Ta = 25 °C		1.40	1.55	1.80	V	
Temperature coefficient of forward voltage		ΔV _F /ΔTa	—	I _F = 10 mA		—	-1.8	—	mV/°C	
Input reverse current		I _R	—	V _R = 5 V, Ta = 25 °C		—	—	10	μA	
Input capacitance		C _T	—	V _F = 0 V, f = 1 MHz, Ta = 25 °C		—	60	—	pF	
Output current (Note 1)	"H" Level	I _{OPH1}	1	V _{CC} = 15 V I _F = 10 mA	V ₆₋₅ = 4 V	—	-0.5	-0.2	A	
		I _{OPH2}			V ₆₋₅ = 10 V	—	—	-0.4		
	"L" Level	I _{OPL1}	2	V _{CC} = 15 V I _F = 0 mA	V ₅₋₄ = 2 V	0.2	0.5	—		
		I _{OPL2}			V ₅₋₄ = 10 V	0.4	—	—		
Output voltage	"H" Level	V _{OH}	3	V _{CC} = 10 V	I _O = -100 mA, I _F = 10 mA	6.0	8.4	—	V	
	"L" Level	V _{OL}			4	I _O = 100 mA, V _F = 0.8 V	—	0.3		1.0
Supply current	"H" Level	I _{CCH}	5	V _{CC} = 10 to 20 V V _O = Open	I _F = 10 mA	—	1.5	3.0	mA	
	"L" Level	I _{CCCL}			6	I _F = 0 mA	—	1.5		3.0
Threshold input current		L → H	I _{FLH}	—	V _{CC} = 15 V, V _O > 1 V		—	1.0	7.5	mA
Threshold input voltage		H → L	V _{FHL}	—	V _{CC} = 15 V, V _O < 1 V		0.8	—	—	V
Supply voltage		V _{CC}	—	—		10	—	30	V	

*All typical values are at Ta=25°C.

Note: This product is more sensitive than conventional products to electrostatic discharge (ESD) owing to its low power consumption design. It is therefore all the more necessary to observe general precautions regarding ESD when handling this component.

Note 1: Duration of I_O time ≤ 50 μs, 1 pulse

Isolation Characteristics (Ta = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance input to output	C _S	V _S = 0 V, f = 1MHz (Note 1)	—	0.8	—	pF
Isolation resistance	R _S	R.H. ≤ 60 %, V _S = 500 V (Note 1)	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 60 s	3750	—	—	V _{rms}

Note 1: This device is regarded as a two terminal device: pins 1 and 3 are shorted together, as are pins 4, 5 and 6.

Switching Characteristics (NOTE)(Ta = -40 to 100 °C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit		
Propagation delay time	L → H	t _{PLH}	7	V _{CC} = 20 V R _g = 30 Ω C _g = 1 nF F = 250 kHz Duty = 50 %	Ta = 25 °C I _F = 0 → 10 mA	—	120	170	ns	
	H → L	t _{PHL}			Ta = 25 °C I _F = 10 → 0 mA	—	120	170		
	L → H	t _{PLH}			I _F = 0 → 10 mA	50	120	200		
	H → L	t _{PHL}			I _F = 10 → 0 mA	50	120	200		
Propagation delay skew (Note 1)		t _{psk}			I _F = 0 ↔ 10 mA	-85	—	85		
Switching time dispersion		t _{PHL} -t _{PLH}			I _F = 0 ↔ 10 mA	—	5	50		
Output rise time (10–90 %)		t _r			I _F = 0 → 10 mA	—	35	—		
Output fall time (90–10 %)		t _f			I _F = 10 → 0 mA	—	15	—		
Common mode transient immunity at HIGH level output		CM _H	8	V _{CM} = 1000 V _{p-p} V _{CC} = 20 V Ta = 25 °C	I _F = 10 mA V _{O (min)} = 16 V	-15	—	—	kV/μs	
Common mode transient immunity at LOW level output		CM _L			I _F = 0 mA V _{O (max)} = 1 V	15	—	—		

(*): All typical values are at Ta = 25 °C.

Note: A ceramic capacitor (0.1 μF) should be connected from pin 6 (V_{CC}) to pin 4 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: Propagation delay skew is defined as the difference between the largest and smallest propagation delay time (i.e. t_{PHL} or t_{PLH}) of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc.).