- **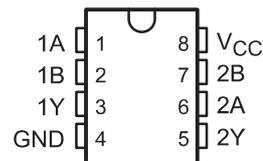Package Options Include Plastic Small-Outline (D, NS, PS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

- **Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package**
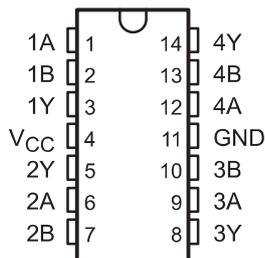
SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74S00 . . . D, N, OR NS PACKAGE
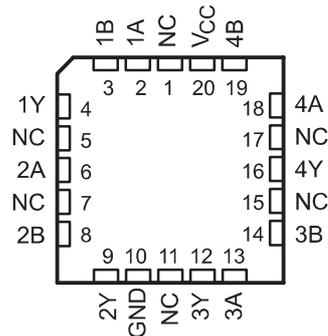SN74LS00 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y
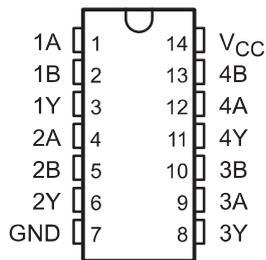
SN74LS00, SN74S00 . . . PS PACKAGE
(TOP VIEW)

1A	1	8	V_{CC}
1B	2	7	2B
1Y	3	6	2A
GND	4	5	2Y

SN5400 . . . W PACKAGE
(TOP VIEW)

1A	1	14	4Y
1B	2	13	4B
1Y	3	12	4A
V_{CC}	4	11	GND
2Y	5	10	3B
2A	6	9	3A
2B	7	8	3Y

SN54LS00, SN54S00 . . . FK PACKAGE
(TOP VIEW)

1Y	4	18	4A
NC	5	17	NC
2A	6	16	4Y
NC	7	15	NC
2B	8	14	3B

Top: 1B 1A NC V_{CC} 4B (3 2 1 20 19)
Bottom: 2Y GND NC 3Y 3A (9 10 11 12 13)

NC − No internal connection

description/ordering information

These devices contain four independent 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

ORDERING INFORMATION

T$_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP − N	Tube	SN7400N	SN7400N
			SN74LS00N	SN74LS00N
			SN74S00N	SN74S00N
	SOIC − D	Tube	SN7400D	7400
		Tape and reel	SN7400DR	
		Tube	SN74LS00D	LS00
		Tape and reel	SN74LS00DR	
		Tube	SN74S00D	S00
		Tape and reel	SN74S00DR	
	SOP − NS	Tape and reel	SN7400NSR	SN7400
			SN74LS00NSR	74LS00
			SN74S00NSR	74S00
	SOP − PS	Tape and reel	SN74LS00PSR	LS00
			SN74S00PSR	S00
	SSOP − DB	Tape and reel	SN74LS00DBR	LS00
−55°C to 125°C	CDIP − J	Tube	SNJ5400J	SNJ5400J
			SNJ54LS00J	SNJ54LS00J
			SNJ54S00J	SNJ54S00J
	CFP − W	Tube	SNJ5400W	SNJ5400W
			SNJ54LS00W	SNJ54LS00W
			SNJ54S00W	SNJ54S00W
	LCCC − FK	Tube	SNJ54LS00FK	SNJ54LS00FK
			SNJ54S00FK	SNJ54S00FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines
are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram, each gate (positive logic)

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