

HEF4011B

Quad 2-input NAND gate

Rev. 6 — 10 December 2015

Product data sheet

1. General description

The HEF4011B is a quad 2-input NAND gate. The outputs are fully buffered for the highest noise immunity and pattern insensitivity to output impedance.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B
- Inputs and outputs are protected against electrostatic effects

3. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
HEF4011BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram

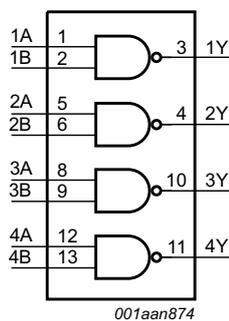


Fig 1. Functional diagram

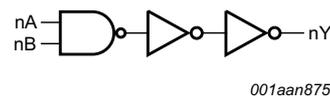
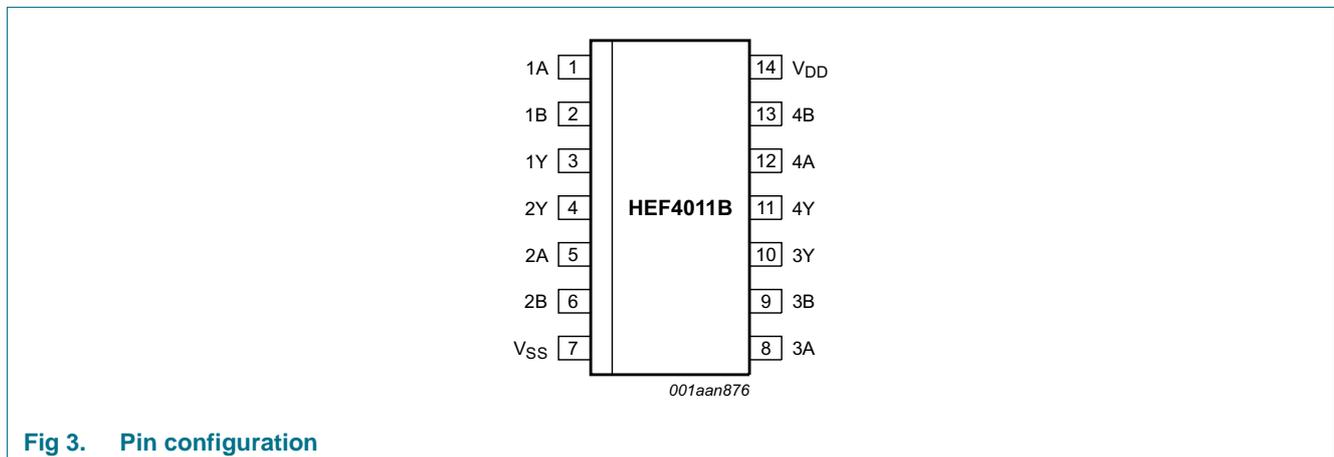


Fig 2. Logic diagram (one gate)

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
nA	1, 5, 8, 12	input
nB	2, 6, 9, 13	input
nY	3, 4, 10, 11	output
V _{SS}	7	ground (0 V)
V _{DD}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level.