

CD4020B, CD4024B, CD4040B Types

CMOS Ripple-Carry Binary Counter/Dividers

High-Voltage Types (20-Volt Rating)

- CD4020B — 14 Stage
- CD4024B — 7 Stage
- CD4040B — 12 Stage

■ CD4020B, CD4024B, and CD4040B are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

The CD4020B and CD4040B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4040B type also is supplied in 16-lead small-outline packages (M and M96 suffixes).

The CD4024B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

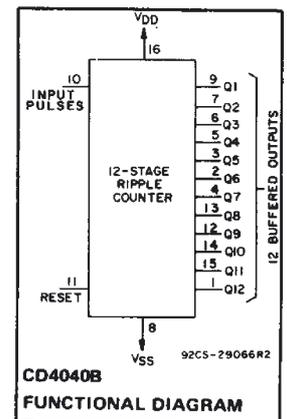
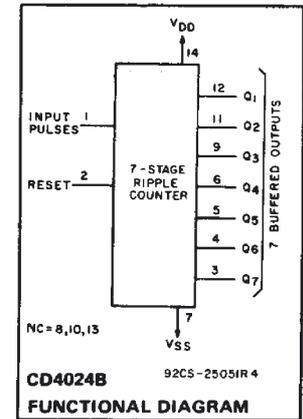
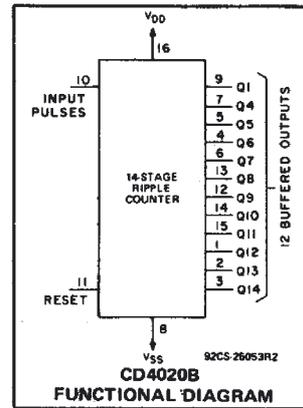
| | |
|---|-------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) | |
| Voltages referenced to V _{SS} Terminal | -0.5V to +20V |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | ±10mA |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -55°C to +100°C | 500mW |
| For T _A = +100°C to +125°C | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | +265°C |

Features:

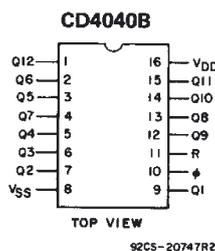
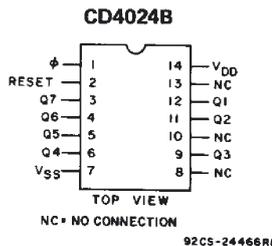
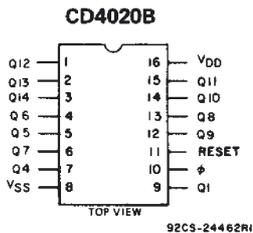
- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- Fully static operation
- Common reset
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
 - 1 V at V_{DD} = 5 V
 - 2 V at V_{DD} = 10 V
 - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits



TERMINAL ASSIGNMENTS



CD4020B, CD4024B, CD4040B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Unless Otherwise Specified
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | | V_{DD} | Min. | Max. | UNITS |
|--|------------------------|---------------|-------------------|----------------|---------------|
| Supply Voltage Range (at $T_A = \text{Full Package-Temperature Range}$) | | | 3 | 18 | V |
| Input-Pulse Frequency, | f_ϕ | 5 10 15 | — — — | 3.5 8 12 | MHz |
| Input-Pulse Width, | t_W | 5 10 15 | 140 60 40 | — — — | ns |
| Input-Pulse Rise or Fall Time, | $t_{r\phi}, t_{f\phi}$ | 5 10 15 | Unlimited | | μs |
| Reset Pulse Width, | t_W | 5 10 15 | 200 80 60 | — | ns |
| Reset Removal Time, | t_{REM} | 5 10 15 | 350 150 100 | — | ns |

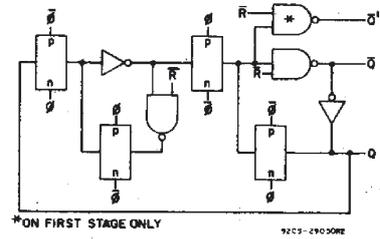


Fig. 4 — Detail of typical flip-flop stage.

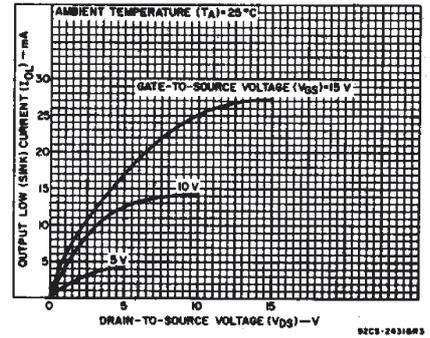


Fig. 5 — Typical output low (sink) current characteristics.

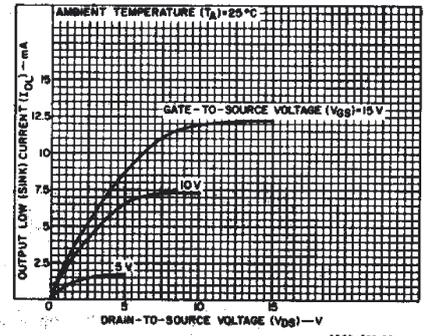


Fig. 6 — Minimum output low (sink) current characteristics.

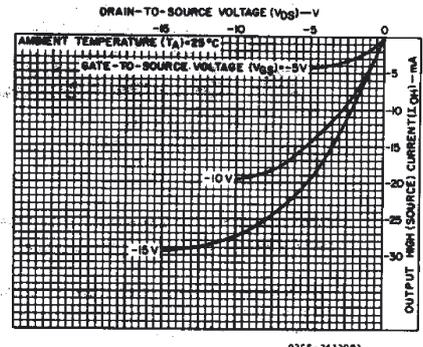


Fig. 7 — Typical output high (source) current characteristics.

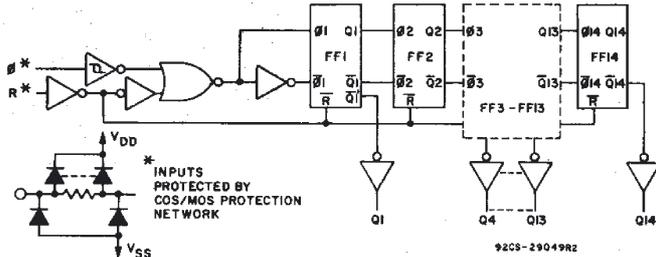


Fig. 1 — Logic diagram for CD4020B.

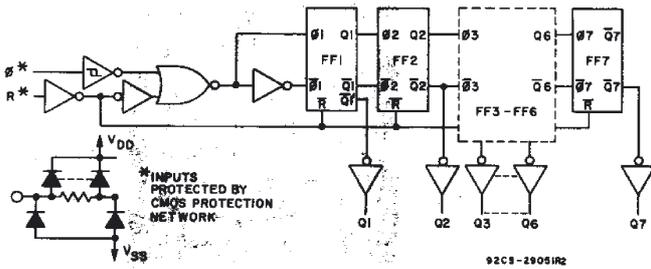


Fig. 2 — Logic diagram for CD4024B.

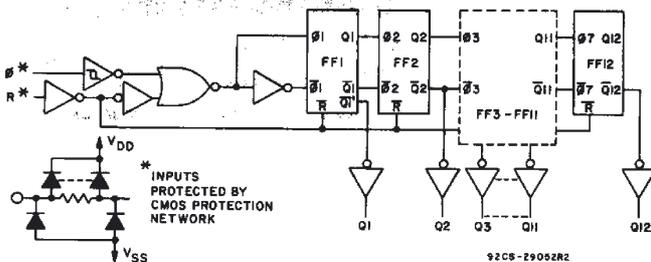


Fig. 3 — Logic diagram for CD4040B.

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 COMMERCIAL CMOS
 HIGH VOLTAGE ICs