

# Critical Conduction Mode PFC IC

## FA1A60N

### Datasheet

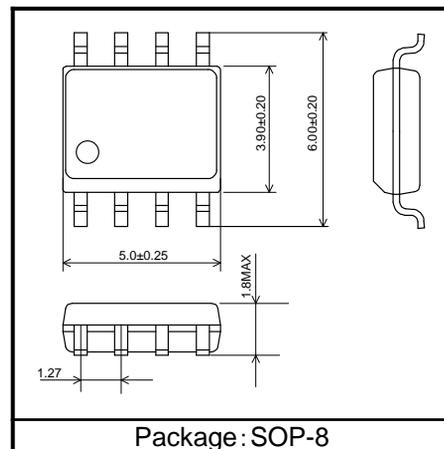
#### 1. Overview

FA1A60N is a power factor correction control IC operating in critical conduction mode. It realizes low power consumption by high voltage CMOS process. It is equipped with many functions such as frequency reduction, FB short protection and double OVP function.

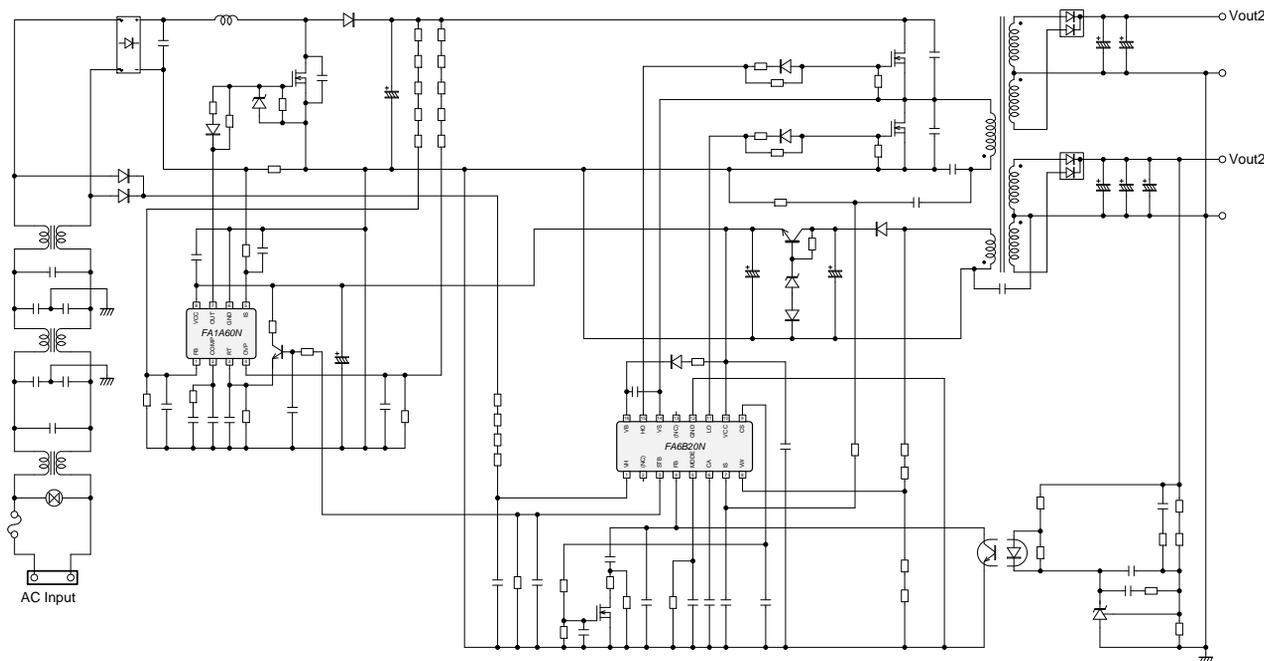
In addition, it includes communication function with Fuji LLC control IC "FA6B20N". It helps to improve efficiency of PSU, to optimize the PFC operation and to reduce external components, if both IC is combined.

#### 2. Features

- Operating mode can be switched between burst mode and normal mode by communication signal from "FA6B20N". It helps to improve light load efficiency.
- Combining with "FA6B20N", operation is optimized according to line voltage and distortion of line current is improved for wide input voltage range.
- Low standby power due to no input voltage detection resistors
- High-precision over current protection:  $0.6V \pm 2\%$
- Improved power efficiency at light load by frequency reduction
- Reduced audio noise at start up by overshoot reduction and dynamic OVP
- Low current consumption by CMOS process,  
Start-up:  $250\mu A$ (typ.), Operating:  $0.8mA$ (typ.)
- Drive circuit for power MOSFET, peak current: source 500mA, sink 1000mA
- Protects the output electrolytic capacitor by the double OVP function, even if a fault happen in the output detection.
- Short protection at feedback (FB) pin
- Under-voltage Lockout
- Restart timer
- 8-pin package (SOP)



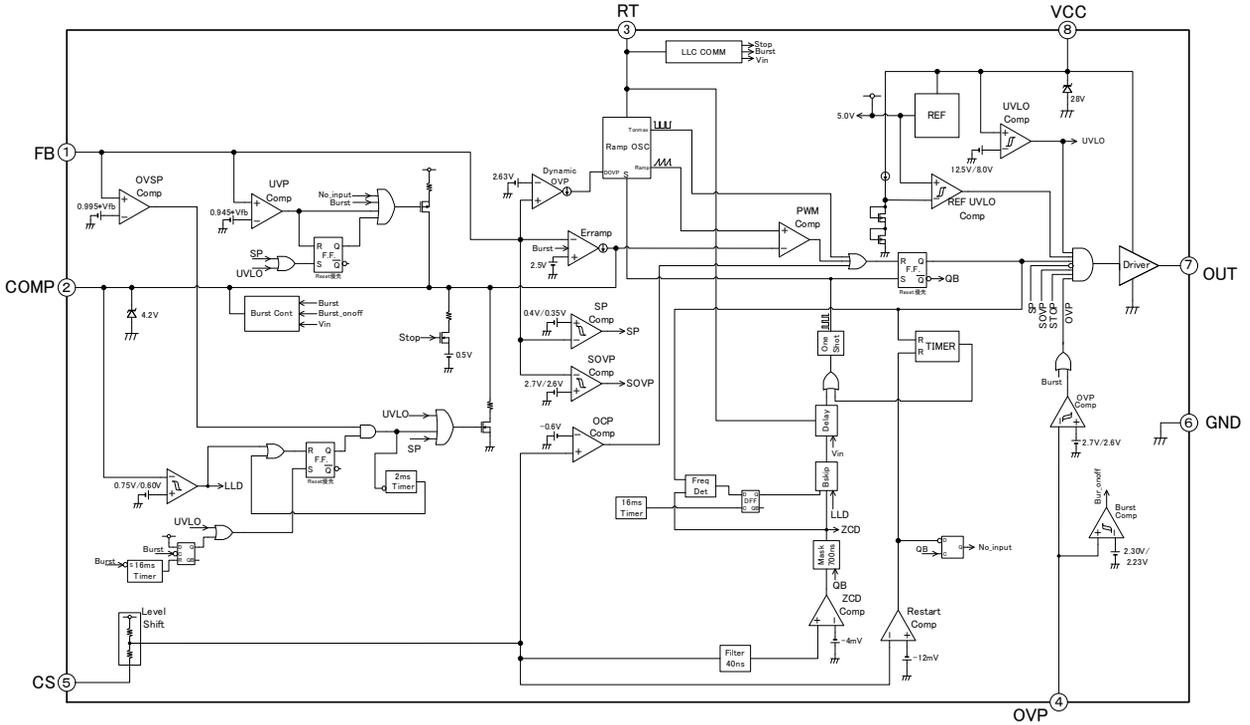
#### 3. Application circuit example (FA1A60N,FA6B20N)



## FA1A60N Datasheet

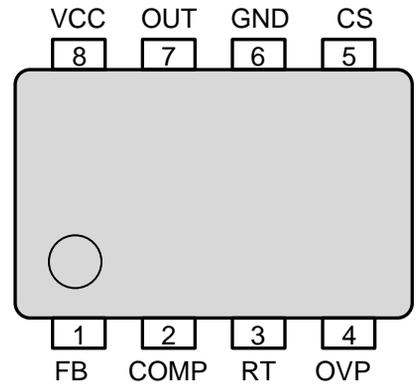
### 4. Block diagram

#### FA1A60N



### 5. Functional description of pins

Pin No.	Pin name	Pin function
1	FB	Feedback control signal input, Short Protection(SP), Dynamic Over Voltage Protection(DOVP), Static Over Voltage Protection(SOVP), Over Shoot Reduction *1
2	COMP	Error amplifier compensation, Burst operation *1
3	RT	Maximum on time and turn on delay setting, Communication with LLC-IC *1,*2
4	OVP	Over Voltage Protection(OVP), Burst operation
5	CS	Current sense input, Frequency reduction, Over Current Protection(OCP) *1
6	GND	Ground
7	OUT	Output
8	VCC	Power supply, Under Voltage Lock Out(UVLO) *1



Notes)

- \*1. Connect capacitor between each pin and GND
- \*2. Connect resistor between each pin and GND

**6. Ratings & characteristics**

Stress exceeding absolute maximum ratings may cause malfunction or damage the device.

“-” shows source and “+” shows sink in current descriptions.

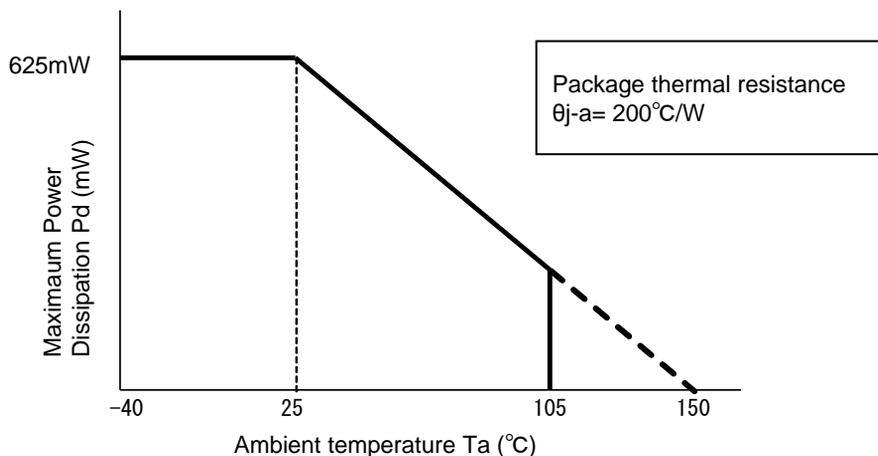
**(1) Absolute maximum ratings**

Item	Symbol	Rating	Unit
Supply voltage *2	VCC	28	V
Voltage inputs(OUT)	Vinout	-0.3 to Vcc+0.3	V
Output peak current source or sink *2 *3	Io	-500 +1000	mA
Voltage inputs(FB)	Vinfb	-0.3 to 5.3	V
Current inputs(FB)	linfb	+100 -100	uA
Voltage inputs(COMP)	Vincomp	-0.3 to 5.3	V
Current inputs(COMP)	lincomp	+100 -100	uA
Voltage inputs(RT)	Vinrt	-0.3 to 5.3	V
Current inputs(RT)	linrt	+100 -100	uA
Voltage inputs(OVP)	Vinovp	-0.3 to 5.3	V
Current inputs(OVP)	linovp	+100 -100	uA
Voltage inputs(CS)	Vincs	-3.3 to 0.3	V
Voltage inputs(CS) at start Up(< 20ms) dV/dt=-10V/100ns *2	Vincs_st	-10 to 0.3	V
Current inputs(CS)	lincs	+100 -100	uA
Current inputs(CS) at start Up(< 20ms) *2	lincs_st	-20 to 0	mA
Power dissipation(Ta=25°C) *2	Pd	625	mW
Operating junction temperature	Tj	-40 to +150	°C
Storage temperature	Tstg	-40 to +150	°C

**Notes)**

\*2: Please consider power supply voltage and load current well and use this IC within maximum temperature in operation. The IC may cross maximum power dissipation at normal operating condition by power supply voltage or load current within peak current absolute maximum rating value.

\*3: The period that exceeds 500mA must be 100ns or less.

**Maximum dissipation curve**


**FA1A60N Datasheet**
**(2) Recommended operating conditions**

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC	10	12	26	V
VCC pin electrolytic capacitor	Cvcc	10	—	47	uF
VCC pin ceramic capacitor	Cvccc	0.1	—	1	uF
Timing resistance	Rrt	20	39	100	kΩ
RT pin capacitor	Crt	0.001	0.01	0.022	uF
Feedback and over voltage detect resistance	Rfb, Rovp	1	—	20	MΩ
CS filter resistance	Rcsf	47	—	100	Ω
Operating ambient temperature	Ta	-40	—	+105	°C

Recommended value is conditions for guaranteeing that the product operates normally.

If it is used out of this condition, there is possibility of have a negative influence on operation and reliability.

Please use it after confirming operation enough with your products when you use it.

**(3) DC electrical characteristics**

The characteristics in this section are those in conditions as follows unless otherwise specified. The voltages described in the conditions are DC input, not AC input.

Vcc=12V, Vfb = 2.4V, Vcomp=4.2V, Rrt= 39kΩ, Vovp=0V, Vcs = +10mV, OUT pin open and Tj = 25°C

Notes)

(1) The item which indicated “\*1” are not 100% tested and guaranteed by design.

(2) “-“ means that it is not guaranteed.

(3) “-“ shows source current and “+” shows sink current in output characteristics.

**6-3-1) Error amplifier (FB pin, COMP pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage feedback input threshold	Vfb		2.475	2.500	2.525	V
Line regulation	Regline	VCC=10V to 26V	-20	-10	+20	mV
Temperature stability *1	VdT	Tj=-30 to 85°C	-	±0.5	-	mV/°C
Transconductance	Gm	VFB(DC)=2.45V, 2.65V, VCOMP(DC)=Vfb Gm=Icomp_2.65- Icomp_2.45/(2.65-2.45)	40	80	120	umho
Output source current	Icompso	VFB(DC)=1.0V VCOMP(DC)=Vfb	-21	-13	-5	uA
Output sink current	Icompsi	VFB(DC)=2.65V, VCOMP(DC)=Vfb	3	11	19	uA
FB pin threshold voltage when COMP pin pull up *2	Vfb_comppull	VFB(DC) decrease VCS(DC)=-20mV	0.925 x Vfb	0.945 x Vfb	0.965 x Vfb	V
COMP pull up resistance when FB pin voltage Decrease *2	Rcomppull	VFB(DC)=2.0V VCOMP(DC)=1.0V VCS(DC)=-20mV	40	50	60	kΩ
COMP clamp voltage when switching stop input	Vclpcomp_stop	VRT pulse H=3.3V	0.45	0.5	0.55	V

\*2: FB pin voltage becomes “FB pin threshold voltage when COMP pin pull up” or less, COMP pin is pulled up by “COMP pull-up resistor when FB pin voltage decrease” (except at startup).

**6-3-2) Ramp oscillator (RT pin, COMP pin, FB pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OUT pin maximum on Time	Tonmax	VFB(DC)=2.4V VCOMP(DC)=4.2V	10	14	18	us
COMP pin threshold voltage for stop switching at OUT pin	Vthcomp	VCOMP(DC) decrease Switching at OUT pin stop	0.5	0.60	0.7	V
COMP pin clamp voltage	Rcomppull	VFB(DC)=1V	4.1	4.2	4.3	V
RT pin output voltage	Vrt	VFB(DC)=2.4V	0.46	0.52	0.58	V

**FA1A60N Datasheet**
**6-3-3) Over voltage comparator (FB pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static OVP threshold voltage	Vsovph	VFB(DC) increase Switching at OUT pin stop	1.060 x Vfb	1.080 x Vfb	1.095 x Vfb	V
	Vsovpl	VFB(DC) decrease Switching at OUT pin start	1.020 x Vfb	1.040 x Vfb	1.060 x Vfb	V
	Vsovphys	Vsovph – Vsovpl	0.030 x Vfb	0.040 x Vfb	0.060 x Vfb	V
Dynamic OVP threshold voltage	Vdovp	VFB(DC) increase Ton=Tonmax x 0.7	1.025 x Vfb	1.050 x Vfb	1.075 x Vfb	V

**6-3-4) Over voltage comparator (OVP pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OVP Pin OVP threshold voltage	Vovph	VOVP(DC) increase Switching at OUT pin stop	1.060 x Vfb	1.080 x Vfb	1.095 x Vfb	V
	Vovpl	VOVP(DC) decrease Switching at OUT pin start	1.020 x Vfb	1.040 x Vfb	1.060 x Vfb	V
	Vovphys	Vovph – Vovpl	0.030 x Vfb	0.040 x Vfb	0.060 x Vfb	V
COMP pin pull down resistance at switching stop	Rcomp_OVP	VOVP(DC)>Vovph VCOMP=1.0V	1.4	2.0	2.6	kΩ

**6-3-5) FB short comparator (FB pin)**

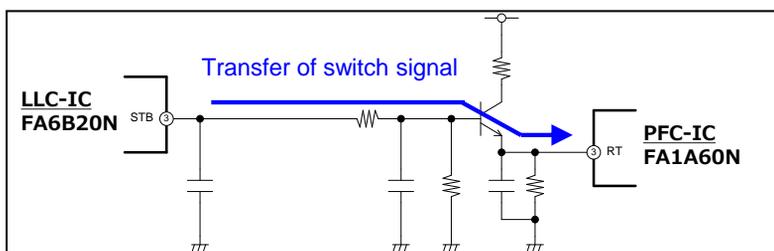
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FB pin threshold voltage	Vthfbh	VFB(DC) increase Switching at OUT pin start	0.36	0.40	0.44	V
	Vthfbl	VFB(DC) decrease Switching at OUT pin stop	0.31	0.35	0.39	V

**6-3-6) Current sense comparator (CS pin, COMP pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CS pin threshold voltage	Vthcsh	VCS(PULSE) : High=10mV Low decrease dV/dT= ±40V/us	-0.612	-0.600	-0.588	V
Temperature stability of CS pin threshold *1	Vthcshdt	Tj=-30°C to 85°C	-1.5	-	+1.5	%
Delay to output	Tphl	VCS(PULSE) : High=10mV Low= -700mV dV/dT= -40V/us VOUT open	50	200	500	ns
Detect voltage of zero current	Vzcd	VCS(DC) increase	-7	-4	-1	mV
Detect delay of zero current	Tzcd	VCS(PULSE) : High=10mV Low= -100mV dV/dT= +40V/us VOUT open Rrt= 39kΩ	0.45	0.9	1.35	us
Masking time of zero current detect after OUT pin turn off	Tmaskzcd	VCS(DC)=10mV Toff(OUT)-Tzcd	0.3	0.7	1.1	us
CS pin source current	Ics	VCS=0V	-10.0	-7.0	-4.0	uA

**FA1A60N Datasheet**
**6-3-7) LLC-IC communication function(1) (RT pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LLC signal1 detect RT pin threshold voltage(change burst/normal operation, input voltage information)	Vthrt_normh	V(RT) pulse increase	1.2	1.4	1.6	V
	Vthrt_norml	V(RT) pulse decrease	0.8	1.0	1.2	V
	Vthrt_normhys	Vthrt_normh - Vthrt_norml	0.2	0.4	0.6	V
LLC signal2 detect RT pin threshold voltage(OUT pin switching stop)	Vthrt_stoph	V(RT) pulse increase	2.8	3.0	3.2	V
COMP pin pull down resistance at switching stop	Rcomp_St	VRT pulse H = 3.3V VCOMP(D) = 1.0V	1.4	2.0	2.6	kΩ
Detecting time of LLC signal1 (Burst↔normal operation)	Thirt	V(RT) pulse>Vthrt_normh	3.2	4.2	5.2	ms
Pulse number of LLC signal1 detect(Vin L →Vin H)	Nrt_vinh	V(RT) pulse>Vthrt_normh	-	1	-	Num
Pulse number of LLC signal1 detect(Vin H →Vin L)	Nrt_vinl	V(RT) pulse>Vthrt_normh	-	2	-	Num
Time up period of LLC signal1 pulse count	Thirt_vin	V(RT) no input after high pulse	5.5	10	15	ms



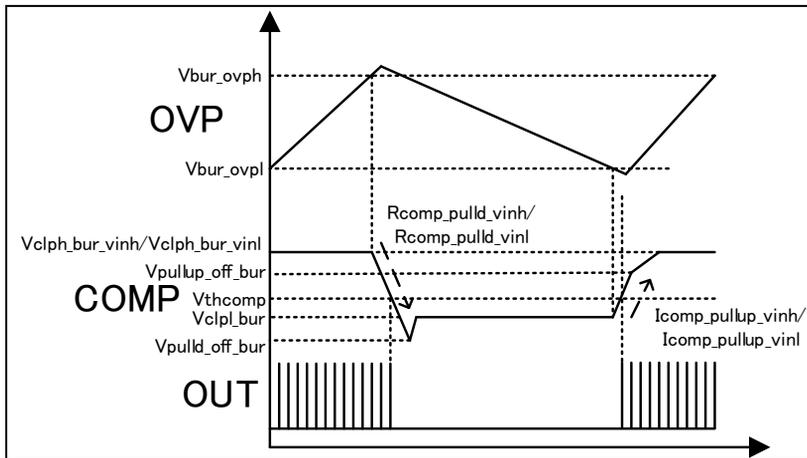
[LLC]STB pin Pulse H level	[LLC]STB pin Pulse width	[LLC]STB pin Number of pulse	[PFC] Operating mode after receipt of signal	Remark
5V	0.25ms	Continues	Stop switching	Interrupt for PFC stop at startup circuit activated or protection
3V	0.5ms	1	Normal operation (HV: high line voltage)	- Switch to normal mode by 0.5ms width signal
		2	Normal operation (LV: low line voltage)	- Setting operating mode for high line or low line by number of pulse
	6ms	1	Burst operation (HV: high line voltage)	- Switch to burst mode by 6ms width signal
		2	Burst operation (LV: low line voltage)	- Setting operating mode for high line or low line by number of pulse

**6-3-8) LLC-IC communication function(2) (RT pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Switch delay of Ramp and Tzcd RT pin threshold voltage	Vrt_swh	V(RT) pulse increase	1.2	1.4	1.6	V
	Vrt_swl	V(RT) pulse decrease	0.8	1.0	1.2	V
	Vrt_swhys	Vrt_swh - Vrt_swl	0.2	0.4	0.6	V
Maximum on time at LLC signal input	Tonmax_rth	V(RT) pulse increase V(COMP)=4.2V	19	27	35	us
ZCD delay at LLC signal input(1st ZCD ON)	Tzcd_rth	V(RT) pulse increase ZCD 1st Bottom	2.4	3.0	3.6	us

**FA1A60N Datasheet**
**6-3-9) Burst control (OVP pin, COMP pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OVP pin burst threshold voltage	Vbur_ovph	VOVP(DC) increase Switching at OUT pin stop	0.89 x Vfb	0.92 x Vfb	0.95 x Vfb	V
	Vbur_ovpl	VOVP(DC) decrease Switching at OUT pin start	0.86 x Vfb	0.89 x Vfb	0.92 x Vfb	V
	Vbur_ovphys	Vbur_ovph – Vbur_ovpl	0.01 x Vfb	0.03 x Vfb	0.05 x Vfb	V
COMP pin clamp voltage at switching in burst mode (Vin L)	Vclph_bur_vinl	VOVP(DC)<0.86xVfb LLC Signal : Vin Low	1.5	1.7	1.9	V
COMP pin clamp voltage at switching in burst mode (Vin H)	Vclph_bur_vinh	VOVP(DC)<0.86xVfb LLC Signal : Vin High	0.65	0.75	0.85	V
COMP pin clamp voltage at switching stop in burst mode	Vclpl_bur	VOVP(DC)>0.95xVfb	0.45	0.5	0.55	V
COMP pin pull up current at switching start in burst mode (Vin L)	Icomp_pullup_bur_vl	VOVP(DC)<0.86xVfb LLC Signal : Vin Low VCOMP(DC)=0.6V	70	100	130	uA
COMP pin pull up current at switching start in burst mode (Vin H)	Icomp_pullup_bur_vh	VOVP(DC)<0.86xVfb LLC Signal : Vin High VCOMP(DC)=0.6V	9	12	15	uA
COMP pin pull up resistance at switching start in burst mode (Vin L)	Rcomp_pullup_bur_vl	VOVP(DC)>0.95xVfb LLC Signal : Vin Low VCOMP(DC)=0.6V	6	10	14	kΩ
COMP pin pull up resistance at switching start in burst mode (Vin H)	Rcomp_pullup_bur_vh	VOVP(DC)>0.95xVfb LLC Signal : Vin High VCOMP(DC)=0.6V	15	26	37	kΩ

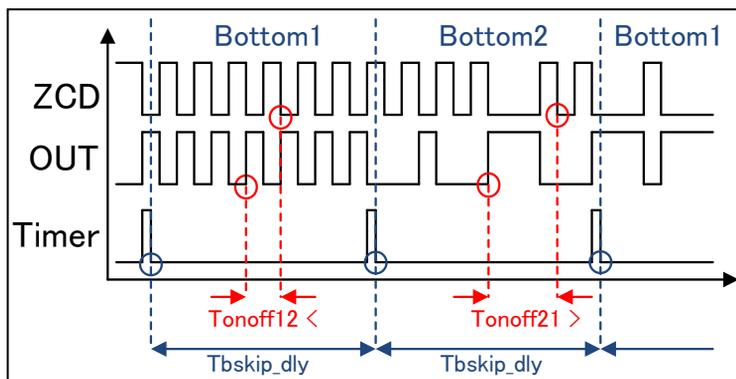


**FA1A60N Datasheet**
**6-3-10) Frequency reduction (CS pin, RT pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Frequency reduction Transition switching period *3	Tonoff12	Bottom1→2	5.6	6.6	7.6	us
	Tonoff21	Bottom2→1	9.0	11.0	13.0	us
OUT pin turn on timer at high input voltage(Bottom 2) *4	Tonbt2_vinh	VCS(PULSE) ZCD time of CS increase OUT pin turn on time from 1st ZCD (Bottom 2) Vin > 170Vac	2.0	2.7	3.4	us
COMP pin threshold voltage for bottom 2	Vthcomp2h	VCS(DC) increase	0.70	0.75	0.8	V
	Vthcomp2l	VCS(DC) decrease	0.55	0.60	0.65	V
Delay time at bottom changing *5	Tbskip_dly	Bottom1⇄2 changeover time	10	16	22	ms

\*3: Switching period (From OUT pin turn on to zero current detection) becomes “Frequency reduction bottom transition switching period” or less, the number of zero current detection until OUT pin turn on increase.

\*4: When OUT pin turn on timer (Bottom ) becomes longer than Restart timer delay, OUT pin turns on Restart timer delay.



\*5: In case that the longest switching period in a period of “Delay time at bottom changing” becomes below “Frequency reduction bottom 1→2 transition switching period”, the timing of turn on changes 1st falling of ZCD to 2nd falling of ZCD. Switching period means the period from rising of OUT to 1st falling of ZCD. In case that the longest switching period in a period of “Delay time at bottom changing period” becomes above “Frequency reduction bottom 2→1 transition switching period”, the timing of turn on changes 2nd falling of ZCD to 1st falling of ZCD.

**6-3-11) Over shoot reduction (FB pin, COMP pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FB pin threshold voltage for over shoot reduction *6	Vthfbovs	VFB(DC) increase	0.96 x vfb	0.98 x vfb	0.995 x vfb	Vfb
Comp pin pull down resistance at over shoot reduction *1 *6	Rcomp_ovs	VFB(DC) increase	1.4	2	2.6	kΩ
Over shoot reduction operation period *1 *6	Tovs	VFB(DC) increase	1	2	3	ms
Over shoot reduction release COMP pin threshold voltage *7	Vcomp_ovsh	VCOMP(DC) increase	0.60	0.75	0.80	V
	Vcomp_ovsl	VCOMP(DC) decrease	0.55	0.60	0.65	V

\*6: At start up, FB pin voltage becomes “FB pin threshold voltage for over shoot reduction” or more, COMP pin is pulled down by “COMP pin pull down resistance at over shoot reduction”.

\*7: “Over shoot reduction operation period” has elapsed or COMP pin voltage becomes “Over shoot reduction release COMP pin threshold voltage”, pull down is released.

**FA1A60N Datasheet**
**6-3-12) Driver output (OUT pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage low state	V <sub>ol1</sub>	V <sub>COMP(DC)</sub> =0V I <sub>sink(OUT)</sub> = 100mA	0.4	1.2	3.3	V
Output voltage low state	V <sub>ol05</sub>	V <sub>COMP(DC)</sub> =0V I <sub>sink(OUT)</sub> = 50mA	0.2	0.6	1.5	V
Output voltage high state *1	V <sub>oh05</sub>	I <sub>source(OUT)</sub> = 50mA	8	9	10	V
Output voltage rise time	T <sub>r</sub>	C(OUT)=1000pF	40	200	600	ns
Output voltage fall time	T <sub>f</sub>	C(OUT)=1000pF	10	50	250	ns

**6-3-13) Restart timer (CS Pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Restart timer delay	T <sub>rest</sub>	V <sub>CS(DC)</sub> =V <sub>thcs_rest</sub>	5	10	15	us
CS threshold voltage at restart timer start	V <sub>thcs_rest</sub>	V <sub>CS(DC)</sub> Increase	-19	-12	-5	mV

**6-3-14) Under voltage lock out (VCC Pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Startup threshold voltage	V <sub>on</sub>	V <sub>CC(DC)</sub> increase Switching at OUT pin start	12.0	12.5	13.0	V
OUT Switching stop threshold voltage	V <sub>off</sub>	V <sub>CC(DC)</sub> decrease Switching at OUT pin stop	7.0	7.5	8.0	V
UVLO hysteresis width	V <sub>hysvcc</sub>	V <sub>on</sub> – V <sub>off</sub>	4.5	5.0	5.5	V

**6-3-15) Power supply current (VCC Pin)**

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Startup power supply current	I <sub>start</sub>	V <sub>CC(DC)</sub> =V <sub>on</sub> -0.1V	150	250	350	uA
Operating power supply current	I <sub>cc</sub>	C <sub>OUT</sub> =OPEN	0.3	0.8	1.3	mA
Dynamic operating power supply current	I <sub>op</sub>	C <sub>OUT</sub> =1000pF	0.5	1.2	1.9	mA
Burst current	I <sub>bur</sub>	Burst mode operation V(OUT) switching stop	150	250	350	uA
Current at switching stop signal	I <sub>stop</sub>	VRT pulse H=3.3V	150	250	350	uA

**7. Characteristics curves**

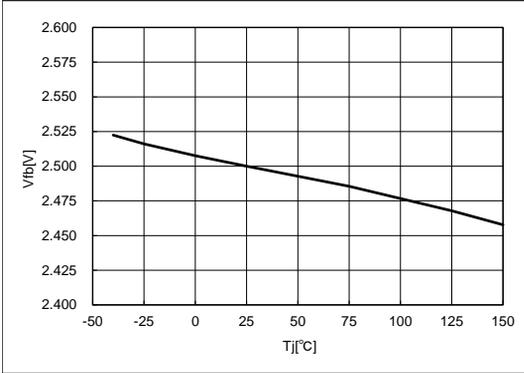
The characteristics in this section are those in conditions as follows unless otherwise specified.

$V_{cc}=12V$ ,  $V_{fb} = 2.4V$ ,  $V_{comp}=4.2V$ ,  $R_{rt}= 39k\Omega$ ,  $V_{ovp}=0V$ ,  $V_{cs} = +10mV$ , OUT pin open and  $T_j = 25^\circ C$

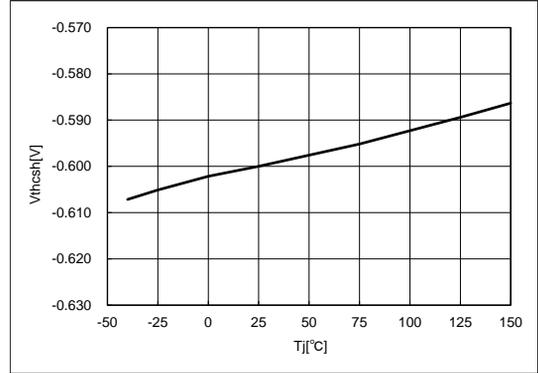
**Notes)**

- (1) “-” shows source current and “+” shows sink current.
- (2) The data listed here show the typical characteristics of an IC and it does not guarantee the characteristic.

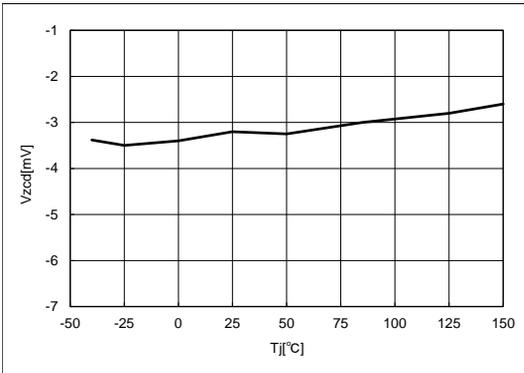
Voltage feedback input threshold ( $V_{fb}$ )  
vs. Junction temperature ( $T_j$ )



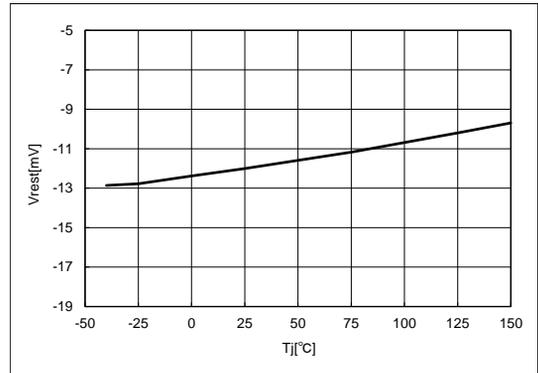
CS pin threshold voltage ( $V_{thcsh}$ )  
vs. Junction temperature ( $T_j$ )



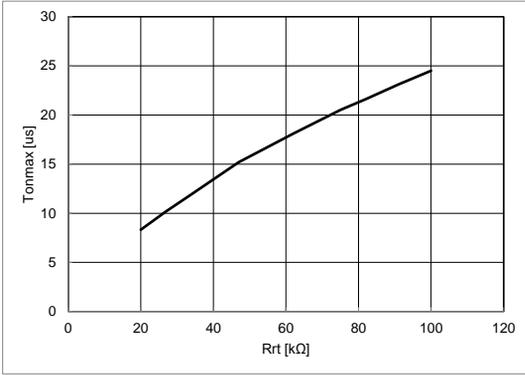
Detect voltage of zero current ( $V_{zcd}$ )  
vs. Junction temperature ( $T_j$ )



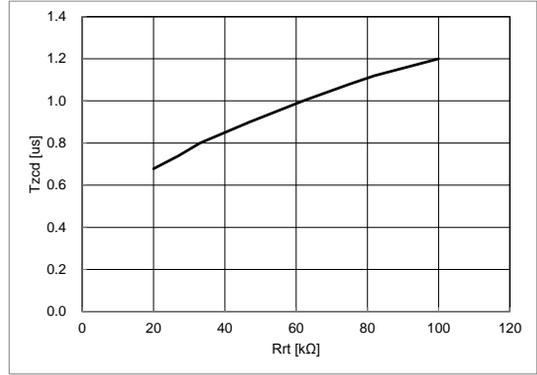
CS threshold voltage at restart timer start ( $V_{thcs\_rest}$ )  
vs. Junction temperature ( $T_j$ )



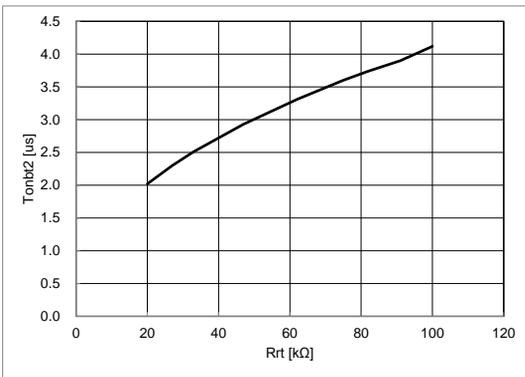
OUT pin maximum on time (Tonmax)  
vs. RT resistance (Rrt)



Detect delay of zero current (Tzcd)  
vs. RT resistance (Rrt)



OUT pin turn on timer of Bottom 2 (Tonbt2)  
vs. RT resistance (Rrt)



**8. Outline of circuit operation**

This IC is a power factor correction controller using boost topology and operating in critical mode. The operations, which are switching operation and power factor correction operation, are described here with the circuit shown in Fig. 1.

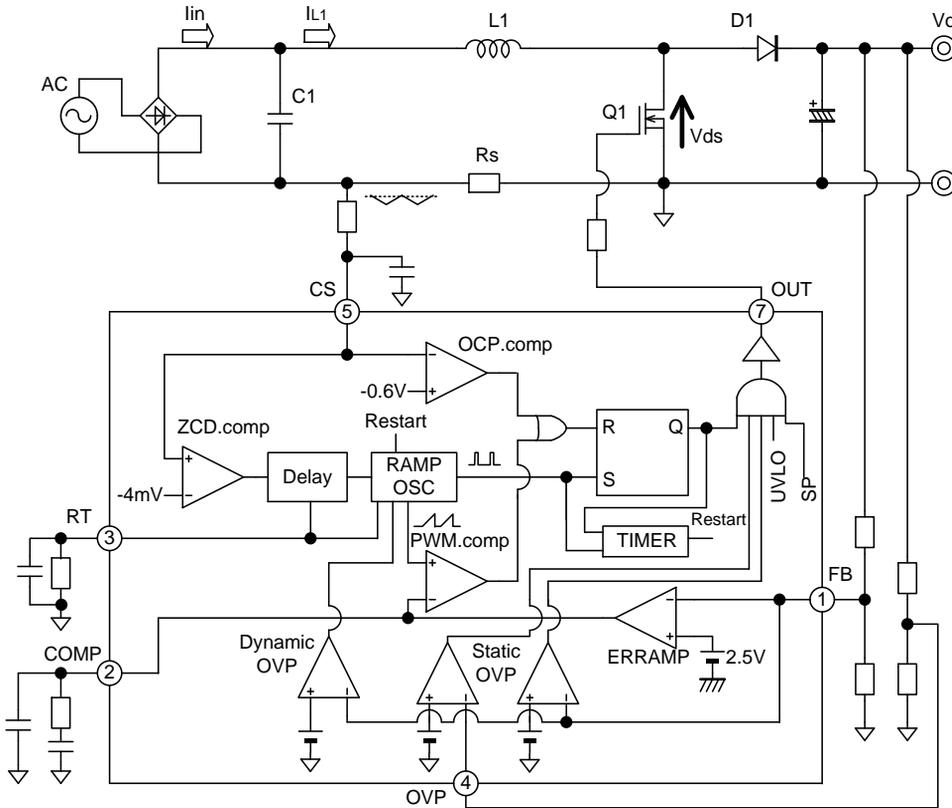


Fig.1 Outline of PFC converter circuit

**(1) Switching operation**

This IC operates in critical conduction mode and does not use a fixed frequency oscillator for switching operation. The waveform of each part in switching operation at steady state is shown in Fig. 2. The operation is as follows.

- [t1]** When Q1 turns on, the inductor (L1) current rises from zero. At the same time, ramp oscillator output  $V_{ramp}$  starts to rise.
- [t2]** Ramp oscillator output  $V_{ramp}$  and the error amplifier output  $V_{comp}$  are compared by the PWM comparator. When  $V_{ramp} > V_{comp}$ , Q1 turns off and the output of the ramp oscillator decreases. When Q1 turns off, the L1 voltage inverts and the L1 current decreases supplying current to output through D1.
- [t3]** The L1 current is detected by CS pin. When the current becomes zero, the output of the current detection comparator becomes high and Q1 is turned on with delay. Then next switching cycle starts (return to t1)

By repeating the steps from t1 to t3, the switching operation continues in critical conduction mode.

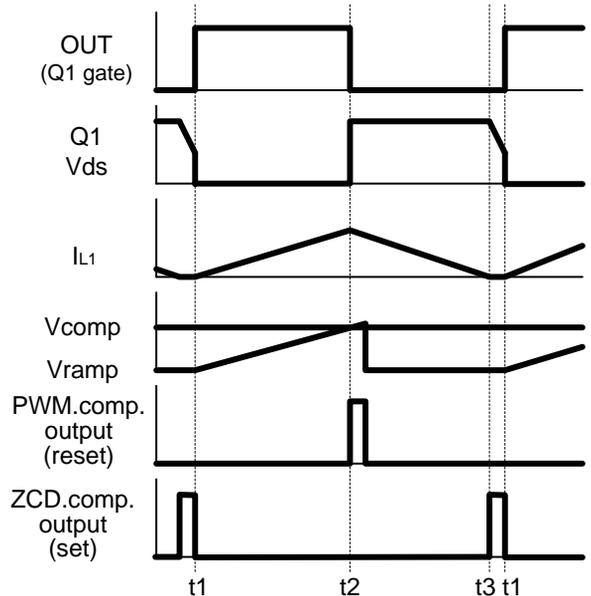


Fig.2 Timing chart of switching operation

As for the PFC converter with critical conduction mode, the switching frequency always changes according to the instantaneous AC line voltage. In addition, the switching frequency also changes when the AC line voltage or the load changes.

**(2) Power factor correction operation**

As explained in the switching operation, the inductor current repeats in triangular waveforms. The mean value ( $I_{L1(\text{mean})}$ ) of the triangular current becomes 1/2 of the peak value ( $I_{L1(\text{peak})}$ ). (Fig. 3) By controlling the peak current of the inductor as sine waveform and removing switching ripple current, the smoothed current flowing from the AC line will be sine waveform.

FA1A60N employs fixed on time control as shown in Fig. 4.

This control determines the on width of the out pulse (gate drive signal for Power MOSFET) using the error amplifier output and saw tooth waveform. When the load is constant, the output of the error amplifier is constant, and on width also stays constant. Since the gradient of the inductor current depends on input voltage (the gradient of inductor current is proportional to input voltage) and on width is constant, the inductor peak current becomes sine waveform same with AC line voltage. As the result, power-factor is corrected.

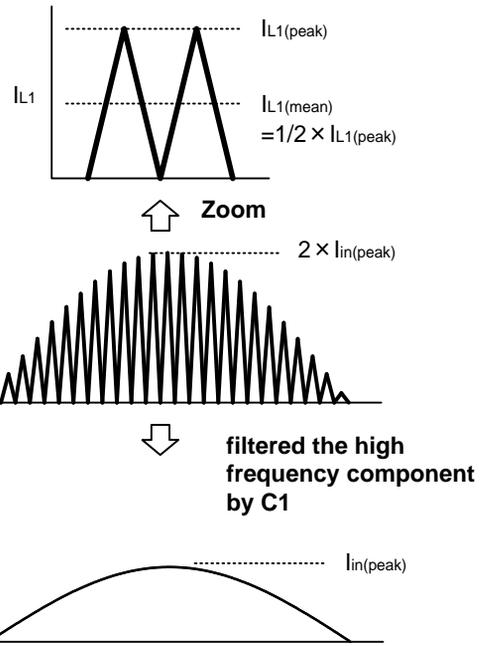


Fig.3 Outline of inductor and AC input current

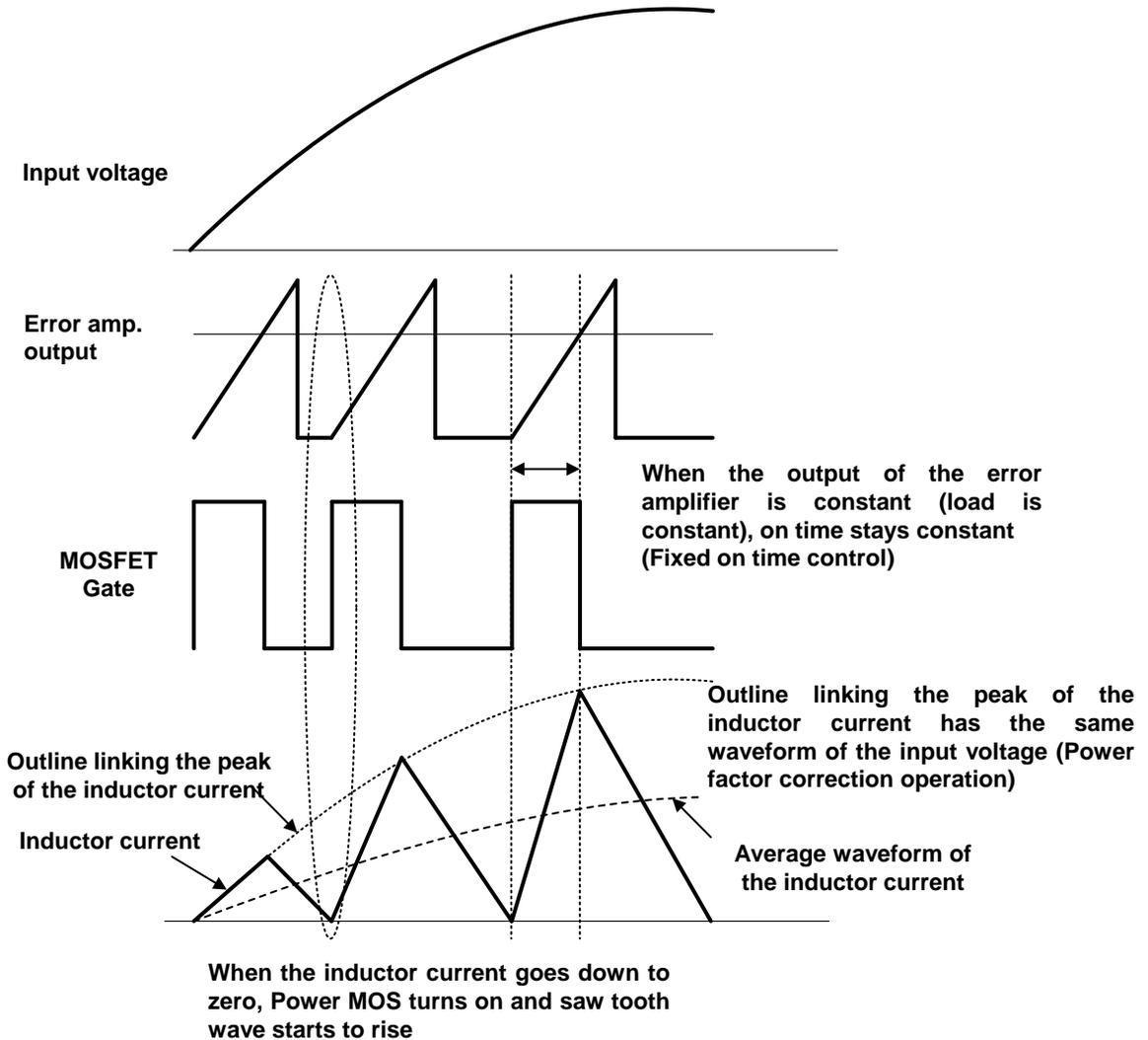


Fig.4 Fixed on time control

**9. Description of each circuit block**
**(1) Error amplifier**

The error amplifier is to make the output voltage constant with feedback control. The amplifier is a transconductance type, which has constant voltage to current gain. The non-inverting input is connected to internal reference voltage of 2.5V (typ.). The inverting input is connected to FB pin and monitors the output voltage of PFC converter. Generally, PFC output voltage is connected to FB pin through resistor divider.

The output of the error amplifier (COMP pin) is connected to the PWM comparator and controls the ON width of the OUT pulse.

The output voltage of PFC contains much of ripple of frequency 2 times AC power line (50 or 60Hz). If large ripple component appears in the output of the error amplifier, the PFC does not stably operate. In order to obtain the stable operation, connect capacitors and a resistor at Pin No. 2 (COMP) as shown in Fig.5.

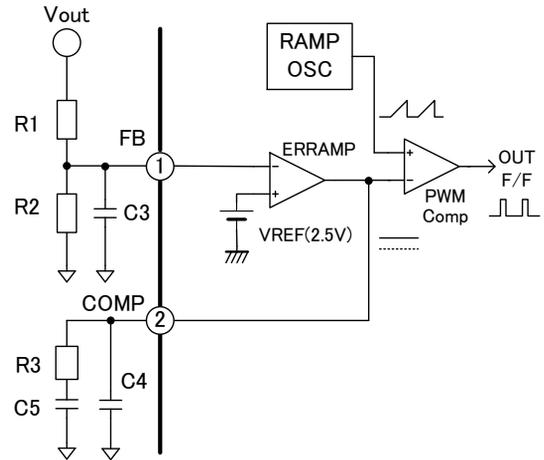
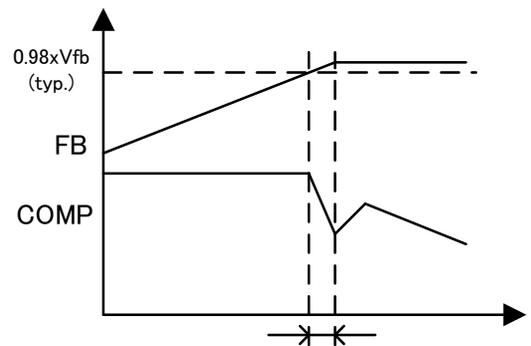


Fig.5 Error amplifier circuit

**(2) Overshoot reduction circuit**

To suppress the overshoot of output voltage at startup, the FA1A60N has an overshoot reduction function. When the output voltage starts increasing after the UVLO or standby mode is reset and reaches the overshoot reduction operation start FB pin voltage ( $0.98 \times V_{fb}$ (typ.)), the overshoot reduction circuit pulls down the COMP pin voltage in short time and limits the ON width of the OUT pin. Thereby it suppresses the increase in the output voltage and reduce overshoot (Fig. 6).

Once the overshoot reduction is operate, it does not operate unless it is reset by the UVLO or standby mode.



Overshoot reduction operation (Pull down COMP)

Fig.6 Overshoot reduction operation

**(3) Overvoltage protection circuit (OVP)**

This circuit limits the PFC output voltage when the output voltage exceeds the programmed voltage.

At startup or dynamic load change, the output voltage of the converter may exceed the set value. In such a case, this protection circuit operates to limit the output voltage.

FA1A60N has 2 types of OVP function as shown below.

- It controls the ON width linearly when the output exceeds the reference voltage.  
Dynamic OVP - - - Built-in FB pin
- It stops the output pulse when the output exceeds 1.08(typ.) times of reference voltage.  
Static OVP - - - Built-in FB pin and OVP pin

The operation of FB pin which has both OVP functions is described below.

FB pin voltage is usually 2.5V as same as the reference voltage. At the startup or a dynamic load change, overshoot appears on PFC output voltage and FB pin voltage will exceed 2.5V. In this case, dynamic OVP function limits ON width depending on FB pin voltage. If FB pin voltage rises more and exceeds a reference voltage of comparator ( $V_{fb} \times 1.08$ (typ.)), static OVP operates and stops the output pulse during exceeding the reference. (Fig.7)

When FB pin voltage decreases to 1.04(typ.) times of reference voltage or lower, IC outputs pulses again.

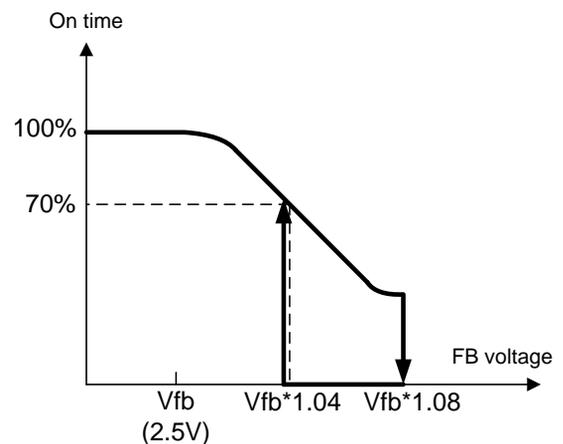


Fig.7 ON width at over voltage

**(4) FB short-circuit detection circuit**

In the PFC circuit of boost type, if FB pin cannot monitor the PFC output voltage due to short-circuit of R2 or open-circuit of R1, the error amplifier cannot control the output voltage and the output voltage abnormally rises. In such a case, the overvoltage protection circuit also cannot operate because the output voltage does not monitored.

To avoid such situation, this IC is equipped with FB short-circuit detection circuit.

This circuit is composed of the reference voltage and comparator (SP). When the input voltage of the FB pin becomes 0.35V(typ.) or lower due to such trouble as short-circuit of R2 or opening of R1, the output of the comparator (SP) inverts to stop the output of the IC and the IC stops operation resulting in standby state.

Once the voltage of the FB pin decreases to almost zero and the output of the IC stops, and then when the voltage of the FB pin returns to 0.4V(typ.) or higher, the IC resumes from the standby state and the OUT pulse restarts.

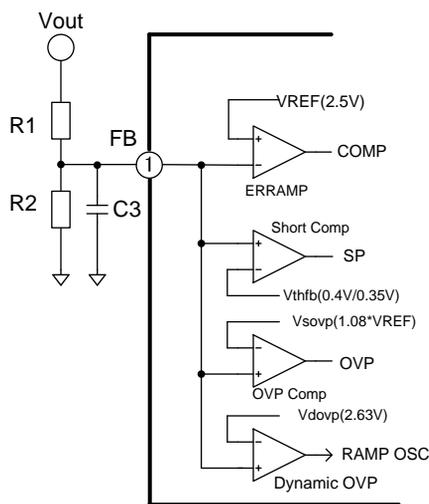


Fig.8 FB pin circuit

**(5) Current detection circuit**

The current detection circuit is composed of zero current detection and overcurrent detection. (Fig.9)

**(5-1) Zero current detection circuit**

This IC operates in critical conduction mode (CRM) by self-oscillation without a fixed frequency oscillator. The zero current detection circuit ZCD comp detects that the inductor current becomes zero to operate in CRM.

The voltage across the current sense resistor  $R_s$  connected to the GND line is input to the CS pin and it is compared by the zero current detection comparator. When CS pin voltage becomes -4mV(typ.) or higher, it judges the inductor current is zero.

After the zero current is detected, the delay  $T_{zcd}$  is generated by the zero cross delay detection circuit, and then set the F/F for OUT to make MOSFET turn on after  $T_{zcd}$ .

**(5-2) Overcurrent detection protective circuit**

When inductor current becomes higher than programmed value, the overcurrent limiting circuit turns off the MOSFET and protects MOSFET. The CS pin voltage compared by the overcurrent detection comparator and it is regarded as overcurrent state when CS pin voltage becomes lower than -0.6V(typ.). When the overcurrent is detected, the F/F for output is reset and the MOSFET is turned off.

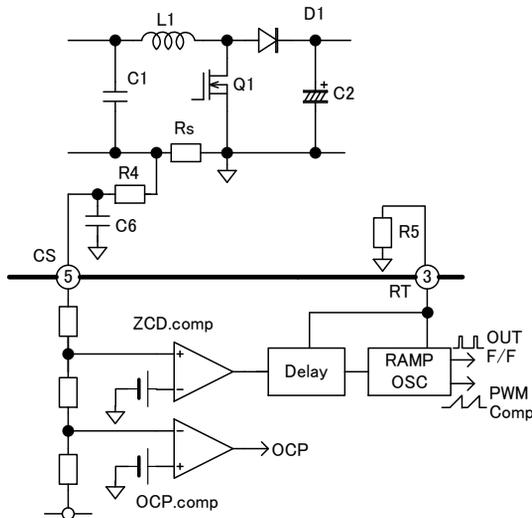


Fig.9 Current detection circuit

**(6) Zero cross delay time setting circuit**

After the inductor L1 current decreases to zero, Vds of the MOSFET starts oscillation due to the resonance of L1 and the parasitic capacitor component on the circuit. MOSFET(Q1) turns on after the inductor L1 current decreases to zero. At that time, with the proper Rrt, MOSFET is turned on at the bottom of the voltage oscillation. This makes it possible to minimize the switching loss and the surge current at the turn-on. (Fig. 10)

If the Rrt is smaller, the turn-on timing becomes earlier and with larger Rrt the turn-on timing is delayed. (Fig. 11)

Since the optimum value of Rrt depends on the circuit and input/output conditions, decide Rrt by evaluating on actual circuit so as to achieve an optimum condition.

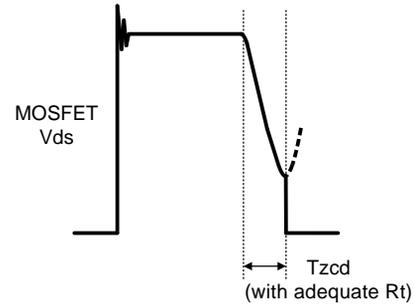


Fig.10 Vds waveform at turn on with adequate Rrt)

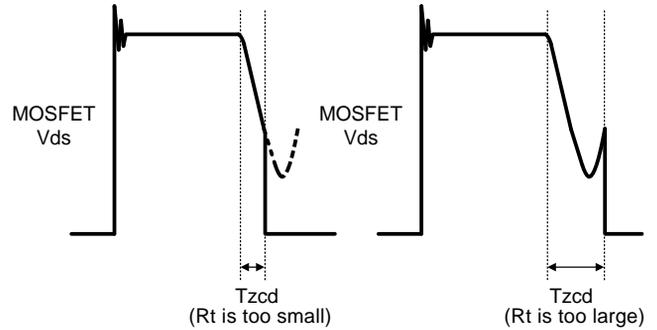


Fig.11 Vds waveform at turn on (with inadequate Rrt)

**(7) Ramp oscillator**

The ramp oscillator receives signal from the zero current detection circuit or restart circuit, and outputs the set signal of F/F for out pulse and saw tooth wave signal for the PWM comparator to decide pulse width.

**(7-1) Frequency reduction function**

The CRM\_PFC mode has characteristics that its switching frequency increases under light load.

FA1A60N limit the increase of frequency and improves the efficiency at light load. The period from the time when the MOSFET turns ON (High of OUT pin) to the time when zero current is detected by the CS pin, which named ON/OFF period Tonoff, is measured and the MOSFET ON timing is determined depending on the Tonoff

If load condition is heavy and Tonoff is larger than 11us, the frequency reduction function does not operate. Under this condition, as shown in Fig. 12, zero current of inductor is detected and MOSFET turns on after delay of Tzcd so as to turn on at the bottom of Vds.

When load is reduced, Tonoff decreases and switching frequency goes high. When Tonoff decreases below 6.6us, as shown in Fig.13, turn on point is switches from 1st bottom to 2nd bottom and the rise of switching frequency is limited.

Threshold of Tonoff for frequency reduction has hysteresis as below.

- Frequency reduction function operating

【1st bottom ⇒ 2nd bottom】  
Tonoff < Tonoff12: 6.6us(typ.)

【2nd bottom ⇒ 1st bottom】  
Tonoff > Tonoff21: 11us(typ.)

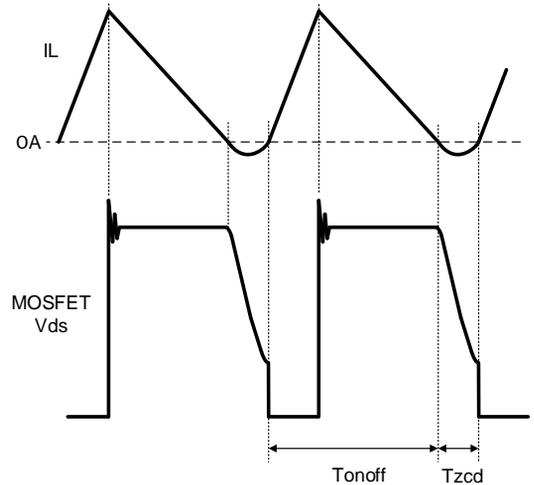


Fig.12 Waveform when the frequency reduction function is not operating. (at heavy loads)

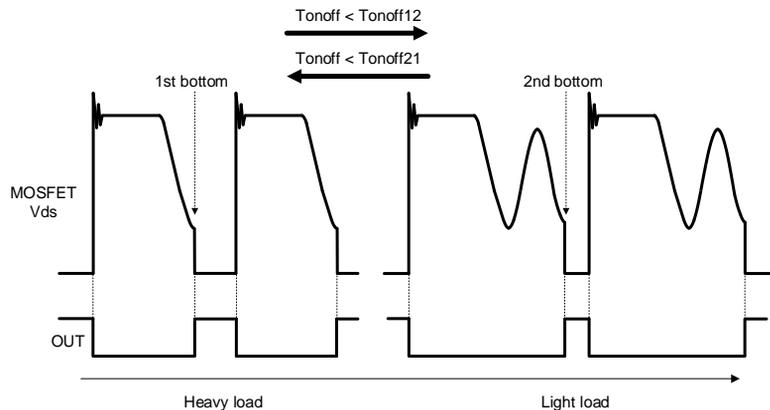


Fig.13 Waveform when the frequency reduction function is operating.

**FA1A60N Datasheet**

Tonoff is monitored for each “Delay time at bottom changing” of 16ms(typ.) and the longest Tonoff is measured in each 16ms. (It appears at almost high phase angle.)

If the measured Tonoff is smaller than “Frequency reduction transition switching period” Tonoff12 of 6.6us(typ.), the IC operates in 2nd bottom switching at next 16ms period.(Fig.14) If the measured Tonoff is larger than “Frequency reduction transition switching period” Tonoff21 of 11us(typ.), the IC operates in 1st bottom switching at next 16ms period.(Fig.15)

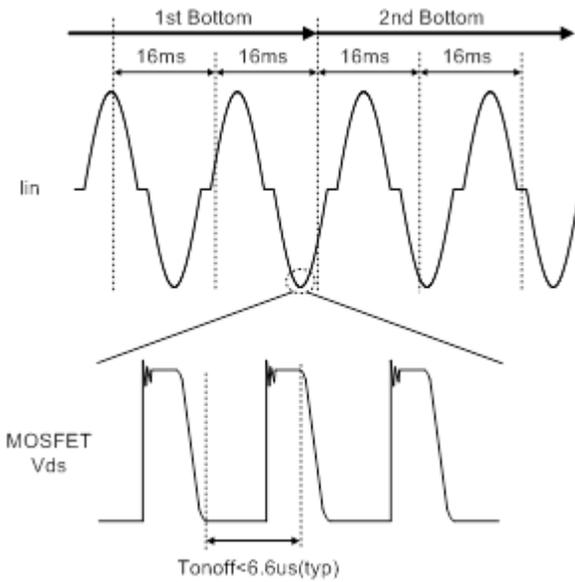


Fig.14 frequency reduction detection 1st→2nd

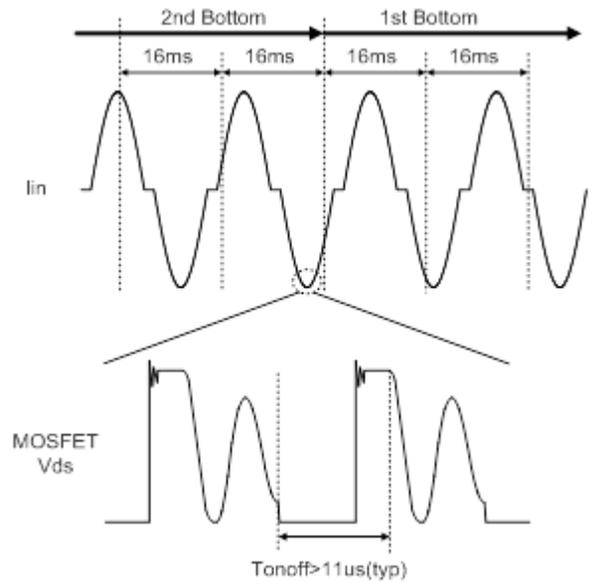


Fig.15 frequency reduction detection 2nd→1st

**(7-2) Line current distortion improvement at high line voltage (turn on timer)**

Combining with LLC\_IC “FA6B20N”, FA1A60N can reduce distortion on line current at high line voltage. As shown in Fig.16, when frequency reduction function operates, MOSFET turns on after 2nd ZCD with delay of Tzcd. However, current oscillation just before turn on is small and 2nd ZCD may not be detected at high line voltage as shown in Fig.17. If 2nd ZCD cannot be detected, MOSFET is turned on with restart timer (10us). It causes line current distortion. To prevent such distortion, FA1A60N receives line voltage information from “FA6B20N” and turns on the MOSFET with turn on timer (Tonbt2\_vinh) after 1st ZCD at high line voltage.

The delay of turn on timer (Tonbt2\_vinh) depends on the RT pin resistor Rrt.

In case of low line voltage, current oscillation just before turn on is relatively large and 2nd ZCD can be detected. Therefore, turn on timer is disabled by the signal from “FA6B20N” at low line voltage.

If FA1A60N does not be combined with “FA6B20N”, FA1A60N is set to low line operation and turn on timer is disabled even in case of high line voltage. It may cause line current distortion at high line voltage.

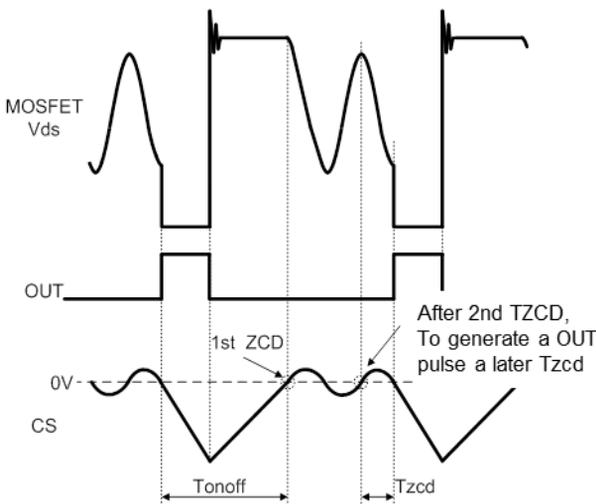


Fig.16 2nd bottom operation waveform

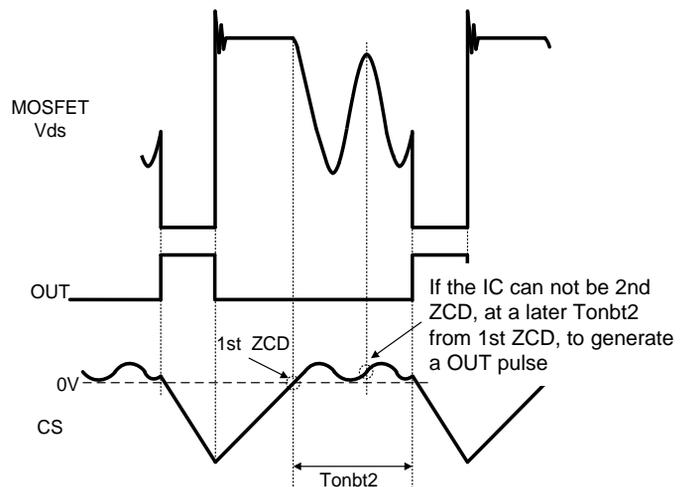


Fig.17 Turn-on timer operation waveforms

**(7-2) 2nd bottom operation by COMP pin voltage**

In case of CRM PFC, Tonoff becomes longer at high line voltage. Therefore, frequency reduction function may not operate at high line voltage.

To prevent such situation, FA1A60N includes switch to 2nd bottom operation by COMP pin voltage. When COMP pin voltage drops below  $V_{thcomp2l}$  of 0.6V(typ.), the IC switches from 1st bottom to 2nd bottom operation. When COMP pin voltage rises over  $V_{thcomp2h}$  of 0.75V(typ.) and  $Tonoff > 11\mu s$ (typ.), the IC switches from 2nd bottom to 1st bottom operation.

**(8) Restart timer**

This IC employs self-oscillation method instead of the fixed frequency with oscillator, and in the steady operation, MOSFET is turned on with a signal from the zero current detector.

However, a trigger signal is required for starting up or stable operation at light load.

This IC is equipped with a restart timer. When a state where OUT pin is low and CS pin voltage is above -12mV continues for 10 $\mu s$ , internal trigger signal generates and OUT pin goes high automatically. This signal can realize stable operation even when starting up or the load is light.

**(9) Under voltage lock out (UVLO)**

UVLO is equipped to prevent circuit malfunction when Vcc voltage drops. When the Vcc voltage rises from zero, the operation starts at 12.5V (typ.). When the Vcc voltage decreases after the operation starts, IC stops the operation at 7.5V (typ.).

**(10) Output circuit**

This IC includes a push-pull drive circuit and can directly drive the MOSFET.

The peak current of the output is 1.0A maximum for sink and 0.5A maximum for source.

**FA1A60N Datasheet**

(11) Communication function with FA6B20N

This IC has a communication function with Current resonant control IC "FA6B20N". The communication signal is sent from STB pin of FA6B20N to RT pin of FA1A60N. PFC operation, such as continuous, burst or stop, is controlled by the signal. In addition, zero current detection is controlled to optimize operation. (FA6B20N: in auto standby operation only)

The merit to control PFC operation by LLC is listed below.

- 1.As for CRM PFC, inductor current is small and switching frequency goes high at light load. Thus, switching loss becomes large and efficiency goes down. With communication function, input power is detected and PFC operation mode is switched from continuous to burst mode. As the result, efficiency at light load is improved.
- 2.LLC part can be started after PFC output voltage rises enough because LLC IC controls PFC operation. It is effective to start up PSU with full load.

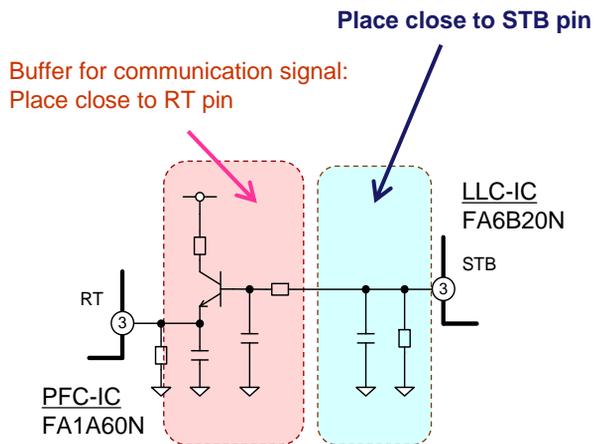


Fig.18 Pin connection for communication function

(11-1) Cooperation between FA6B20N and FA1A60N

Fig.18 shows the circuit diagram of communication between FA6B20N and FA1A60N. FA6B20N detects input power and switches PFC to normal mode or burst mode. FA6B20N transmit the signal from STB pin and FA1A60N receives it at RT pin. As for signal transmission wiring, a buffer circuit for the signal should be inserted close to RT pin of FA1A60N. The communication signals are 5 types as listed in table 1.

Table 1. Communication signal between PFC and LLC

Operating mode	Standby pin output voltage	Signal width	Number of signal
Normal to burst (Vin=100V line)	3V	6ms	2 pulses
Normal to burst (Vin=200V line)	3V	6ms	1 pulse
Burst to normal (Vin=100V line)	3V	0.5ms	2 pulses
Burst to normal (Vin=200V line)	3V	0.5ms	1 pulse
PFC stop	5V	0.25ms	Continuous

(12) Burst operation

When RT pin receives the signal to switch to burst mode from LLC-IC, PFC turns into burst operation. (Fig.19) Instead of FB pin control at normal mode, the output voltage is controlled by OVP pin using hysteresis control with threshold of  $V_{bur\_uvph}/V_{burovpl}$  at burst mode.

FB pin OVP is kept effective at burst mode. If output voltage rises higher than the voltage programed by OVP pin for some reason, FB pin OVP stops switching. Therefore, double OVP system is maintained even in case of burst mode.

2nd OVP voltage at normal mode and output voltage at burst mode is programed by OVP pin resistors  $R_{ovph}$  and  $R_{ovpl}$ . Two comparators with different reference voltage are provided for OVP pin and the comparator is switched depending on the operating mode.

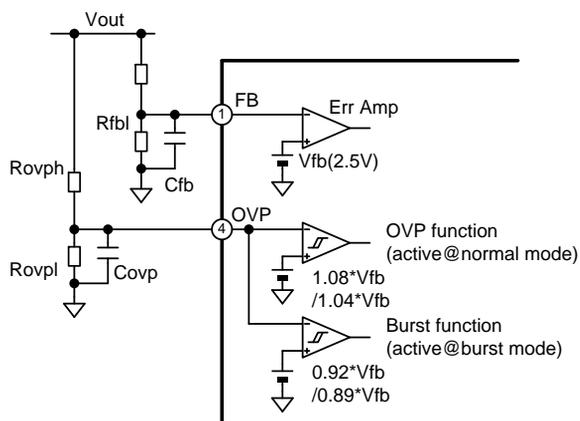


Fig.19 PFC output voltage detection

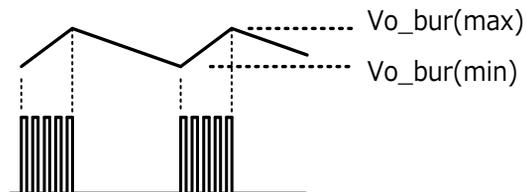


Fig.20 Output voltage at burst mode

### 10. How to use each pin and advice for designing

#### (1) No.1: FB pin

##### 【Functions】

- ( i ) Input of feedback signal for output voltage setting
- ( ii ) Detect short-circuit of FB pin
- ( iii ) Detect output overvoltage

##### 【How to use】

- ( i ) Feedback signal input

##### ✓ Connection method

Connect to output voltage through resistor divider.

##### ✓ Operation

The PFC output voltage  $V_{out}$  is controlled so that FB pin voltage is equal to the internal reference voltage (2.5V(typ.))

$$V_{out} = \frac{V_{REF}}{R2} \times R1 + V_{REF}$$

$V_{REF}$ : Reference voltage=2.5V(typ)

Select below 20MΩ for the resistor divider of FB pin. To prevent malfunction due to noise, capacitor C3 of 1nF to 47nF should be connected between the FB pin and GND. Do not place the resistors near the switching device (MOSFET) to avoid influence of noise.

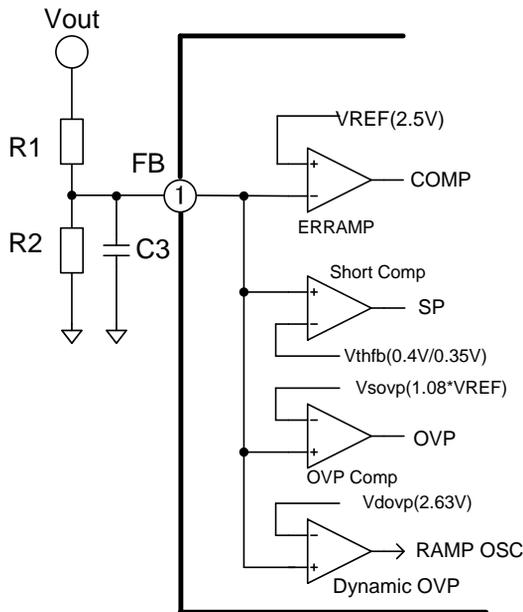


Fig.21 FB pin circuit

- ( ii ) FB pin short-circuit detection

##### ✓ Connection method

Same as for the ( i ) Feedback signal input

##### ✓ Operation

If the input voltage of the FB pin becomes 0.35V or lower due to short-circuit of R2, the output of the comparator (SP) inverts to stop the output of the IC.

- ( iii ) Output overvoltage detection

##### ✓ How to connect

Same as for the ( i ) Feedback signal input

##### ✓ Operation

Normally the voltage of the FB pin is 2.5V almost same as the reference voltage of the error amplifier. If the output voltage rises for some reason and the voltage of the FB pin reaches the comparator reference voltage ( $V_{REF} \times 1.08$ (typ.)), the output of the comparator (OVP) inverts to stop the OUT pulse. If the output voltage returns to the normal value, the OUT pulse resumes.

#### (2) No.2: COMP pin

##### 【Function】

Phase compensation of internal error amplifier

##### 【How to use】

##### ✓ Connection method

Connect C, R between COMP pin and GND as shown in Fig. 22.

##### ✓ Operation

C, R connected to COMP pin suppress the ripple voltage which has 2 times frequency of AC line.

(Reference)

Example of application circuit:

$C4=0.1\mu F$ ,  $C5=1\mu F$ ,  $R3=12k\Omega$

The above is a reference example, and it should be decided by sufficiently evaluation with actual application circuit.

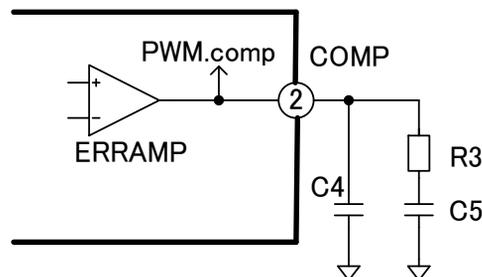


Fig.22 COMP pin circuit

**(3) No.3: RT pin**

**【Functions】**

- ( i )Set maximum ON width
- ( ii )Set delay time for zero current detection
- ( iii)Switch burst mode or normal mode by external signal

**【How to use】**

- ( i ) Set maximum ON width  
ON width  $T_{on}$  in each switching cycle is theoretically expressed by the following formula.

$$T_{on} = \frac{2 \times L_p \times P_o}{V_{ac}^2 \times \eta}$$

Input Voltage (Vrms): Vac  
 Inductor (H): Lp  
 Maximum Output Power (W): Po  
 Efficiency:  $\eta$

The maximum ON width  $T_{onmax}$  must be set larger than the ON width at minimum input voltage Vac (min) at which the ON width is maximum. The maximum ON width should be set as shown by the following formula.

$$T_{onmax} > \frac{2 \times L_p \times P_o}{V_{ac(min)}^2 \times \eta}$$

✓Connection method

Connect R5 between RT pin and GND as shown in Fig.23. As for the resistance dependency of the maximum ON width, see Chapter 7. Characteristic Curve. The source current of RT pin changes depending on the resistor. Connect capacitor C7 of 1nF to 10nF in parallel with the resistor as shown in Fig.23.

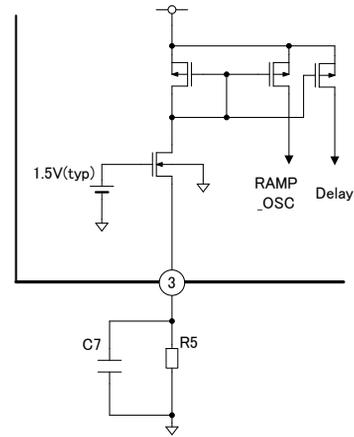


Fig.23 RT pin circuit

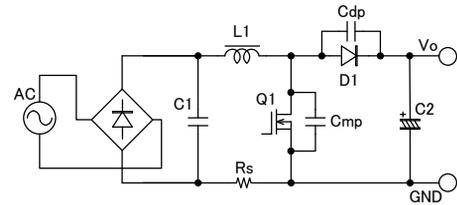


Fig.24 PFC main circuit

- ( ii ) Set delay time for zero current detection

Select a resistance value so that the delay time allows the MOSFET to be turned on at the bottom of Vds. (See Section 9 (6) Zero cross delay time setting circuit.)

Adjustment is normally made at the high line voltage of the AC input voltage range. (Around 240Vac when the voltage ranges from 90Vac to 264Vac). However, smaller resistor makes maximum ON width  $T_{onmax}$  small and maximum output power cannot be output. Do not choose the resistance which gives smaller ON width than the result of above equation for maximum on width. If the delay time is too large, adjust the capacitor Cmp or Cdp in Fig.24 larger to fit the bottom of Vds to the delay time.

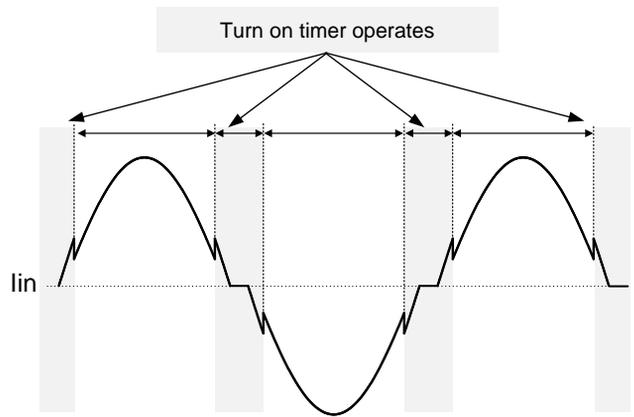


Fig.25 Line current distortion at high line voltage

**【Design advice】**

In case of low line voltage, the line current distortion as shown in Fig.25 does not appear because turn on timer is disabled and 2nd ZCD can be detected.

In case of high line voltage, however, the line current distortion as shown in Fig.25 may appear when frequency reduction function operates (2nd bottom operation). It is because MOSFET is turned on by turn on timer before 2nd ZCD at low phase angle, though by 2nd ZCD at high phase angle.

The distortion can be reduced by using larger Rrt to prolong the turn on timer.

**FA1A60N Datasheet**

(iii) Switch burst mode or normal mode by external signal  
 Operation mode is switched between burst mode and normal mode by external signal. See page 19 “(11) Communication with FA6B20N” for detailed operation.

✓Connection method

As shown in Fig.26, NPN transistor as buffer is connected to RT pin as close as possible in order to prevent influence of noise at communication signal wiring. (Example:  $R_B=1K\Omega$ ,  $C_B=1nF$ ,  $R_C=10K\Omega$ )

✓Operation

LLC IC FA6B20N monitors AC line voltage and load condition, and outputs pulse signal from STB pin. (See page 19 table 1) PFC IC switches operating mode between normal operation and burst operation. See FA6B20N data sheet for details.

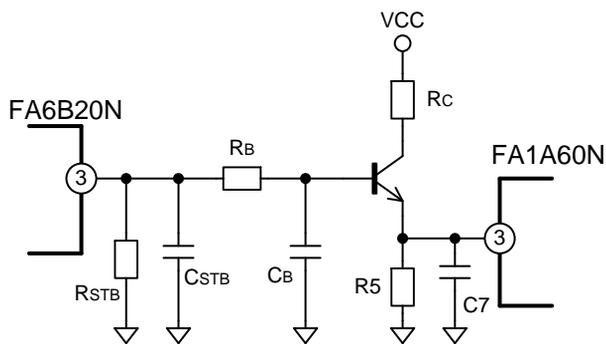


Fig.26 Communication function circuit

**(4) No.4: OVP pin**

**【Function】**

- ( i ) Set overvoltage protection
- ( ii ) Set output voltage at burst mode

**【How to use】**

- ( i ) Set overvoltage protection

✓Connection method

Connect as shown in Fig.27.

✓Operation

It sets a voltage which detects an over voltage of PFC Vo and stop switching operation.

Since the resistors of OVP pin causes power loss, relatively high resistance is recommended.(20MΩmax)

The resistance is calculated by following equation.

$$Rovpl = \frac{Vref \times 1.095 \times Rovph}{Vstop - Vref \times 1.095}$$

Vstop: Overvoltage detection voltage,

Vfb: Reference voltage =2.5V(typ.)

1.095: OVP Ratio to Vfb (max)

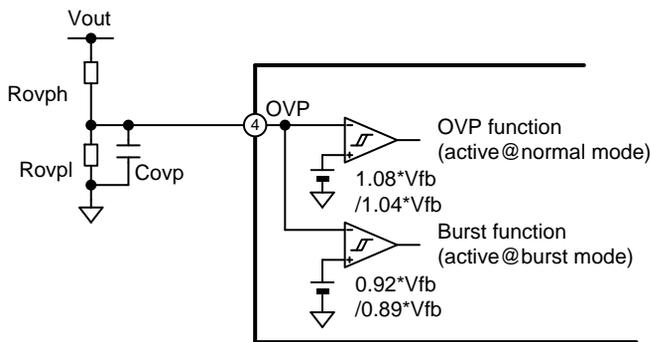


Fig.27 OVP pin circuit

- ( ii ) Set output voltage at burst mode

✓Connection method

Connect as shown in Fig.27.

✓Operation

2nd OVP voltage at normal mode and output voltage at burst mode operates on the basis of OVP pin voltage. Two comparators with different reference voltage are provided for OVP pin and the comparator is switched depending on the operating mode.

Output voltage at burst mode is calculated by following equations.

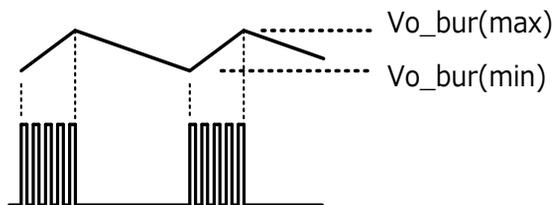


Fig.28 Output voltage at burst mode

OVP voltage

$$Vovp = 1.08 \times 2.5V \times \frac{Rovph + Rovpl}{Rovpl}$$

Burst voltage

$$Vo\_bur(max) = 0.92 \times 2.5V \times \frac{Rovph + Rovpl}{Rovpl}$$

$$Vo\_bur(min) = 0.89 \times 2.5V \times \frac{Rovph + Rovpl}{Rovpl}$$

### (5) No.5: CS pin

#### 【Function】

- ( i ) Detect overcurrent and turn off MOSFET
- ( ii ) Detect zero current of the inductor

#### 【How to use】

- ( i ) Overcurrent protection

##### ✓Connection method

Connect the current sense resistor  $R_s$  between the source terminal of MOSFET (GND) and the minus lead of the input capacitor (C1). The voltage across  $R_s$  is input to the IC as the current signal.

##### ✓Operation

When the CS pin voltage becomes smaller than  $-0.6V$ , the OCP comparator output inverts and MOSFET is turned off.

The maximum threshold voltage  $V_{thcsh}$  of the CS pin is  $-0.588V(max)$ .

The current sense resistor  $R_s$  is set so that maximum current can be supplied with  $V_{thcsh}(max)$ .

With maximum output  $P_o$  (W) and minimum input voltage  $V_{ac}$  (min), the maximum value of peak current ( $I_{LP}(max)$ ) through the inductor can be approximately expressed by the following formula.

$$I_{LP}(max) = \frac{2 \times \sqrt{2} \times P_o}{\eta \times V_{ac}(min)}$$

Therefore, the value of  $R_s$  ( $\Omega$ ) is determined as follows.

$$R_s < \frac{-V_{thcsh}}{I_{LP}(max)} = \frac{0.588}{I_{LP}(max)}$$

- ( ii ) Zero current detection

##### ✓Operation

The CS pin voltage is input to ZCD comparator. When CS pin voltage becomes larger than  $-4mV$ , the comparator output inverts and OUT pin voltage goes high.

#### 【Design advice】

When MOSFET turns on, surge voltage may appear on CS pin due to the gate drive current or discharge of the parasitic capacitors. Large surge voltage may cause malfunction and AC line current may be disturbed. Normally, therefore, a CR filter is connected as shown in Fig.29. The cutoff frequency of this CR filter must be set sufficiently higher than the switching frequency so that it will not affect the normal operation.

It is recommended to set this cutoff frequency to about 1 to 2MHz.

$$\frac{1}{2 \times \pi \times C6 \times R4} \doteq 1 \text{ or } 2[\text{MHz}]$$

Since the CS pin is connected to resistor level shift circuit as shown in Fig.29, filter resistor R4 is recommended to be  $47\Omega$  to  $100\Omega$ .

The maximum rating voltage of the CS pin is  $-10V$  at start up ( $<20ms$ ). In case of boost converter, rush current to charge the output smoothing capacitor C2 flows at the moment the ac input voltage is connected. This current may become far larger in comparison with the input current during normal operation.

As a result, larger voltage may also be applied to the CS pin than the normal current.

If larger voltage than maximum ratings is applied to CS pin due to inrush current, reduce inrush current by inrush current limiting circuit or limit the CS pin voltage by connecting Zener diode as shown in Fig.30, 31. Impedance of wiring to CS pin should be small to prevent the influence of noise that may cause malfunction.

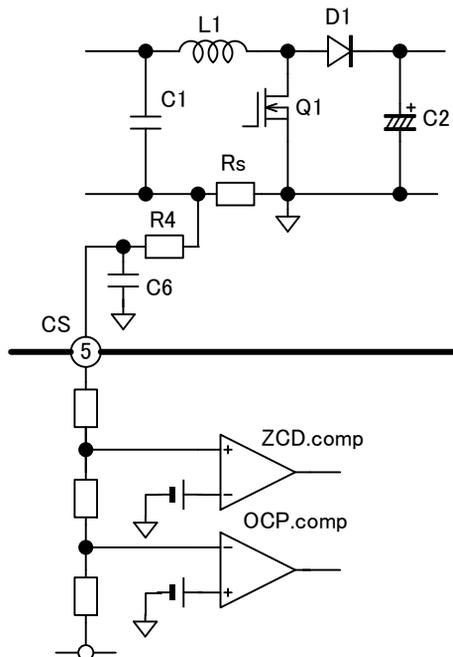


Fig.29 CS pin circuit

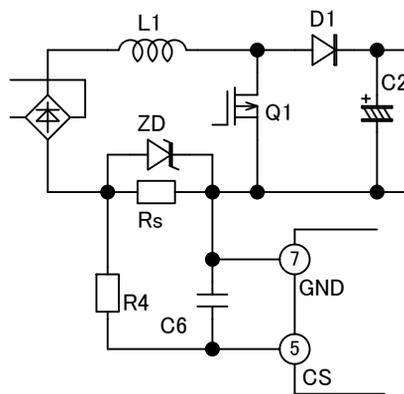


Fig.30 CS pin protection circuit (1)

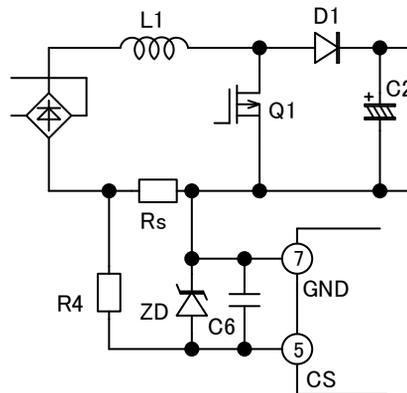


Fig.31 CS pin protection circuit (2)

**(6) No.6 GND pin**
**【Function】**

GND pin is the reference for the voltage of each part of the IC.

**(7) No.7: OUT pin**
**【Function】**

Output of the gate driver for the MOSFET

**【How to use】**
**✓Connection method**

OUT pin is connected to the gate of MOSFET via resistor.

**✓Operation**

During the MOSFET is on, the state is set to high and almost the VCC voltage is output.

During the MOSFET is off, the state is set to low and the voltage of almost 0V is output.

**【Design advice】**

The gate resistor is connected to limit the current of the OUT pin and prevent oscillation of the gate terminal voltage. The rating of the output current is 0.5A for source and 1A for sink.

With the connections shown in Fig.33 or Fig.34, it is possible to independently set the gate driving current of turning on and off MOSFET.

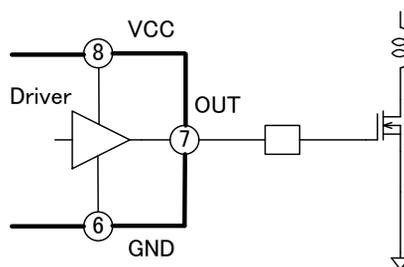


Fig.32 OUT pin circuit (1)

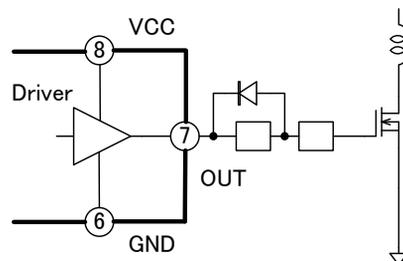


Fig.33 OUT pin circuit (2)

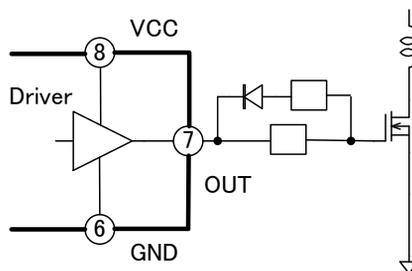


Fig.34 OUT pin circuit (3)

**(8) No.8 VCC pin**
**【Function】**

Supply the power of IC

**【How to use】**
**✓Connection method**

External DC voltage is connected to VCC pin to operate IC. To stabilize VCC voltage, capacitor should be connected to VCC pin as close as possible as shown in Fig.35.

**✓Operation**

Startup threshold voltage of Vcc is 13V(max.). Therefore, External VCC voltage should be higher than 13V. After startup, IC stops operation at 7.5V(typ.) by UVLO function. While the IC stops by UVLO, OUT pin is kept low state.

**【Design advice】**

The current supplied to VCC pin includes MOSFET drive current in addition to IC operating current. Consider the current supply capability of external VCC voltage.

Noise may appear on VCC pin because MOSFET gate drive current is pulse waveform. To suppress the noise, as shown in Fig.35, connect a ceramic capacitor of 0.1uF or larger to VCC pin as close as possible.

In case that the auxiliary winding on PFC inductor is used for VCC voltage, connect as Fig. 36.

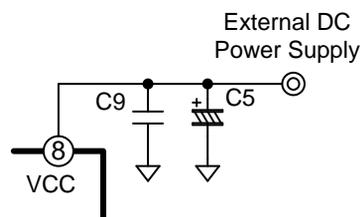


Fig.35 VCC pin circuit(1)

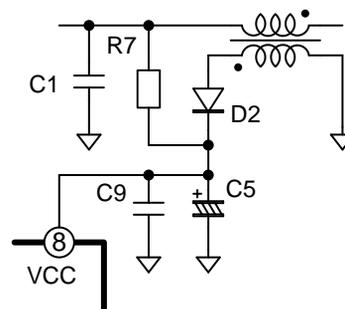


Fig.36 VCC pin circuit(2)

### 11. Advice for design

#### (1) Minus voltage on each pins

In some cases, the voltage oscillation of  $V_{ds}$  just before MOSFET turns on is applied to the OUT pin through parasitic capacitors, etc. and minus voltage may be added to the OUT pin. If this minus voltage is large, the parasitic element inside the IC is activated, and the IC may malfunction.

If this minus voltage exceeds  $-0.3V$ , Schottky barrier diode should be connected between the OUT pin and GND. With the forward voltage of the Schottky barrier diode, the minus voltage can be clamped.

For other pins, care should be taken so that minus voltage will not be applied in the same way.

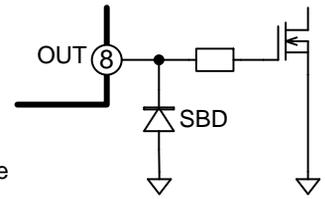


Fig.37 Minus voltage prevention

#### (2) Advice in pattern designing

Main circuit components such as MOSFET, inductor, and diode are operating with large voltage and current. Therefore, if the IC or wiring of input signals are located close to these main circuit components, malfunction may occur due to noise generated there. Special care should be taken to the following cases. (Bad examples)

- IC is placed under the main circuit components such as inductor or just on the back side of the main circuit components. (Fig. 38)
- IC is placed just beside the inductor, MOSFET or diode. (Fig. 39)
- Signal wiring are placed under the inductor or near MOSFET or diode. (Fig. 40)

If the PFC output is connected to the load circuit such as the DC/DC converter, inverter, etc., separate both GND wiring at output capacitor so that GND wiring of the PFC and load circuit does not interfere each other by the switching current. (Fig. 41)

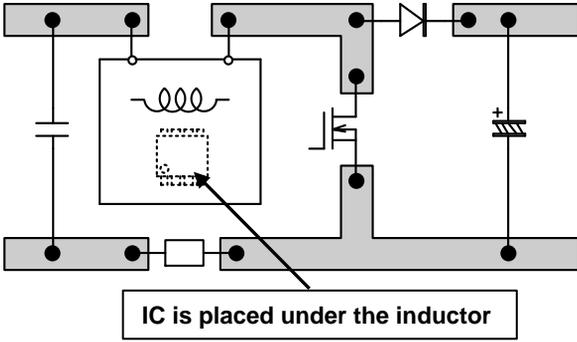


Fig.38 Bad layout example (1)

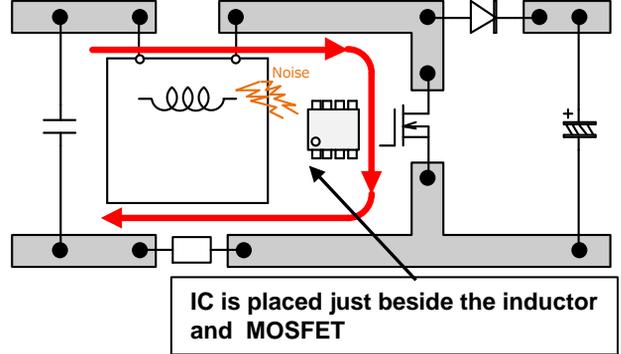


Fig.39 Bad layout example (2)

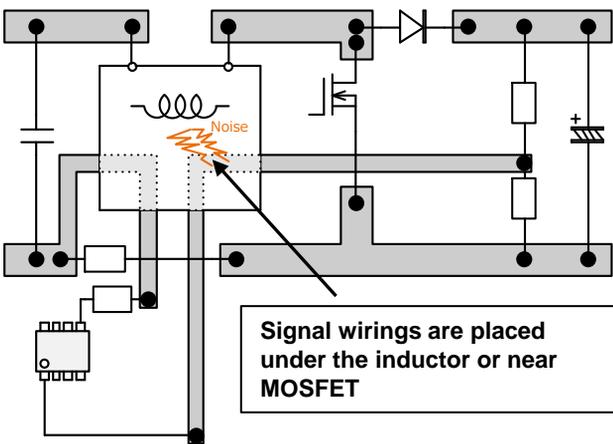
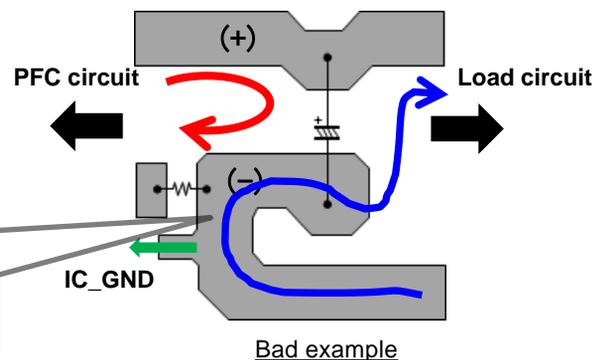
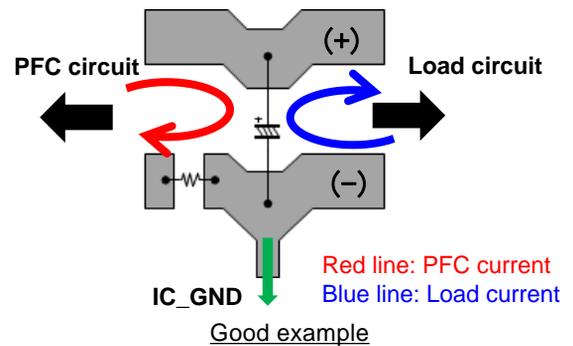


Fig.40 Bad wiring example



PFC current and load current flows common GND wiring.  
↓  
Noise of load current affects PFC current sensing etc.

Fig.41 PFC-Load wiring example

**(2) Example of GND wiring around IC**

To minimize the influence of the main circuit noise to the IC, consider the followings.

- Separate the signal circuit GND and the main circuit GND, and connect both GND at the current sense resistor Rs.(Fig.42)
- The wiring between the CS pin and Rs and between Rs and GND pin should be as short as possible because the CS signal voltage is small and so easily influenced by noise.
- Connect the VCC-GND capacitor close to the IC. The capacitor is used to suppress noise and If the capacitor is placed far away from the IC, its effects are reduced.
- The transistor connected to RT pin should be placed close to the IC and wiring between RT pin and emitter pin of the transistor should be as sort as possible.

(Note)

This wiring example is to make users understand the idea of GND wiring. The noise and malfunction are different depending on each application circuit, and it is not to guarantee that all application circuit will normally operate even if you use this wiring example (Fig. 43)

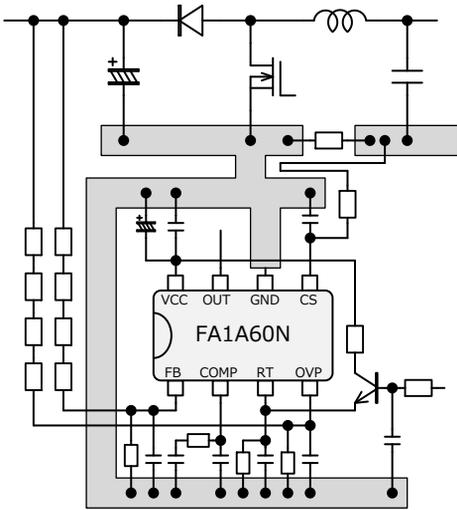


Fig.42 Good example of GND wiring around IC

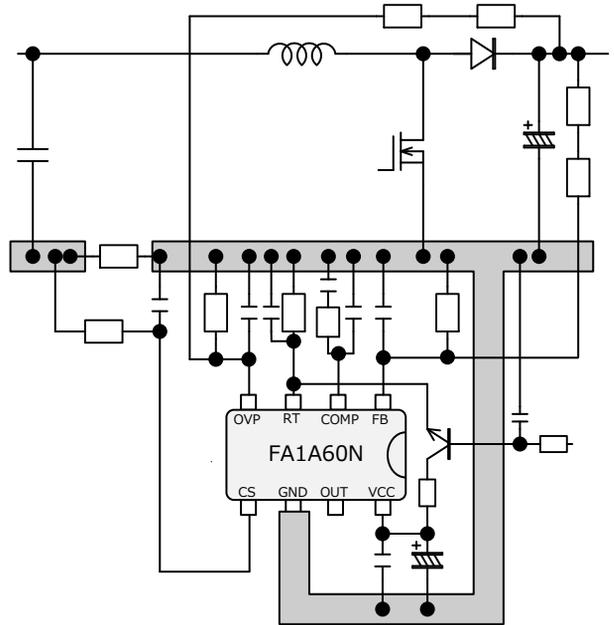


Fig.43 Bad example of GND wiring around IC

**(4) Wiring of the small signal pins**

Wiring of the pins related to small signal (RT, OVP, FB, COMP, CS) should be placed so as not to be affected by OUT pin. Especially, it may cause malfunction that the wiring is placed in parallel with OUT pin wiring. (Fig.44, Fig.45)

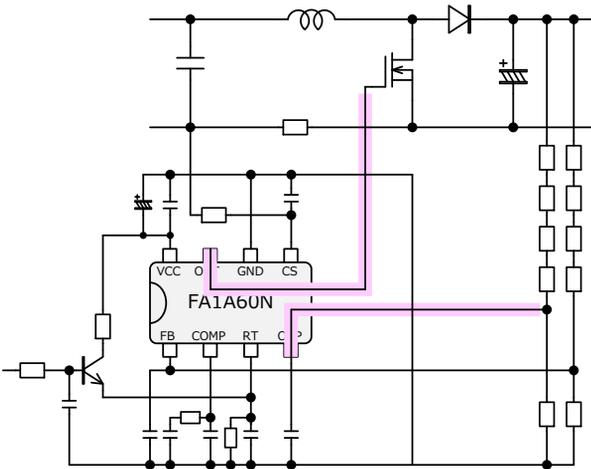


Fig.44 Bad example of the wiring

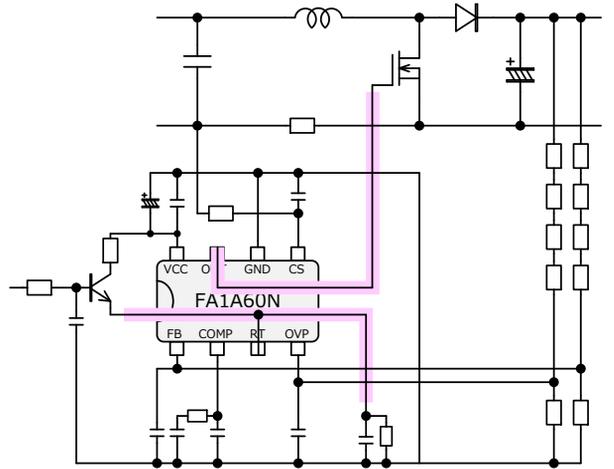


Fig.45 Bad example of the wiring

**FA1A60N Datasheet**
**(3) Cautions in use about pin noise**

When noise is input each pin of IC, IC may malfunction following below. Please confirm that neither the instable operation nor the malfunction occurs by noise and use this IC

Condition	Pin	malfunction in fear	Input regulations	Cautions in design
Start Up	CS	It may not turn on if input voltage less than threshold voltage.	Do input voltage more than threshold voltage	Design the PCB pattern to offset current is not generated in the inductor current sensing line
Input noise (within absolute maximum ratings)	FB	Switching may stop when noise is over OVP level	Input signal is only for feedback voltage of output voltage	Connect capacitor near terminal pin
		IC may become standby mode when noise is under short detection level (after standby mode cancellation become restart)		
		Offset occurs in output voltage and output voltage rises or falls by a noise		
		Output voltage may fall when enter the dynamic OVP domain by a noise		
	COMP	On width may become not constant by load, output may change heavily by a noise	Cancel noise	Confirm sufficiently phase compensation constant
		Switching may become when noise is over threshold voltage		
		Switching may stop when noise is under threshold voltage		
	RT	On width may become not constant by load, output changes heavily by a noise	Cancel noise	Care the pattern of substrate
		Restriction of maximum on time may not work when voltage is higher than pin voltage (On width may change when voltage is higher than pin voltage)		
		On width and restriction may change when voltage is lower than pin voltage		
	OVP	Switching may stop when noise is over OVP level	Cancel noise	Connect capacitor near IC
	CS	Turn-on occurs unintentional timing, Mos/Diode heat and switching noise may become bigger by a noise	Cancel noise	Connect capacitor near pin
		It may not turn on when the time over turn-on threshold is less than delay time	Although Inductor and Mos capacitance is resonant, input voltage more than threshold over delay time	Connect capacitor near pin
		Frequency reduction function may not work when noise frequency is faster than maximum frequency of setting	Cancel noise	Connect capacitor near pin
GND		Reference voltage changes, IC may not behave normally	Cancel noise	Ground wiring should be a wide wiring
OUT		The output may fall not to be able to drive Mos normally when signals more than the ability of the driver are input	Cancel noise	—
VCC	IC may stop when noise under UVLO is input	Don't input noise under UVLO when operating	Connect capacitor near pin	
Input minus voltage (less than absolute maximum voltage)	FB	A parasitism element works, and the malfunction such as IC stop may occur	Don't input minus voltage less than maximum absolute voltage	—
	COMP			
	RT			
	OVP			
	IS	IC may be destroyed		Please put a Diode with a current sense resistor in parallel
	OUT	IC may be destroyed		-
VCC	A parasitism element works, and the malfunction such as IC stop may occur	-		
Input plus voltage (more than absolute maximum voltage)	FB	IC may be destroyed	Don't input plus voltage more than maximum absolute voltage	-
	COMP			
	RT			
	OVP			
	IS	GND level may be changed		
	OUT	IC may be destroyed		
VCC	IC may be destroyed			

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