FAIRCHILD SEMICONDUCTOR®

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FSL106HR
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche-Rugged SenseFET (650V)
- Under 50mW Standby Power Consumption at $265V_{AC}$, No-load Condition with Burst Mode
- Precision Fixed Operating Frequency with Frequency Modulation for Attenuating EMI
- Internal Startup Circuit
- Built-in Soft-Start: 20ms
- Pulse-by-Pulse Current Limiting
- Various Protections: Over-Voltage Protection (OVP), Overload Protection (OLP), Output-Short Protection (OSP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown Function with Hysteresis (TSD)
- Auto-Restart Mode
- Under-Voltage Lockout (UVLO)
- Low Operating Current: 1.8mA
- Adjustable Peak Current Limit

Applications

- SMPS for VCR, STB, DVD, & DVCD Players
- SMPS for Home Appliance
- Adapter

Related Resources

- *AN-4137 — Design Guidelines for Off-line Flyback Converters using FPS™*
- *AN-4141 — Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*
- *AN-4147 — Design Guidelines for RCD Snubber of Flyback*
- *Fairchild Power Supply WebDesigner — Flyback Design & Simulation - In Minutes at No Expense*

Description

The FSL106HR integrated Pulse Width Modulator (PWM) and SenseFET is specifically designed for high-performance offline Switch-Mode Power Supplies (SMPS) with minimal external components. FSL106HR includes integrated high-voltage power switching regulators that combine an avalanche-rugged SenseFET with a current-mode PWM control block.

The integrated PWM controller includes: Under-Voltage Lockout (UVLO) protection, Leading-Edge Blanking (LEB), a frequency generator for EMI attenuation, an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, and temperature-compensated precision current sources for loop compensation and fault protection circuitry. The FSL106HR offers good soft-start performance. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSL106HR reduces total component count, design size, and weight; while increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for the design of cost-effective flyback converters.

Maximum Output Power[1]			
$230V_{AC}$ ± 15%[2]		$85\text{-}265V_{AC}$	
Adapter[3]	Open Frame	Adapter[3]	Open Frame
9W	13W	8W	10W

Notes:
1. The junction temperature can limit the maximum output power.
2. $230V_{AC}$ or $100/115V_{AC}$ with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FSL106HR	-40 to 105°C	FSL106HR	8-Lead, Dual Inline Package (DIP)	Rail

Pin Configuration

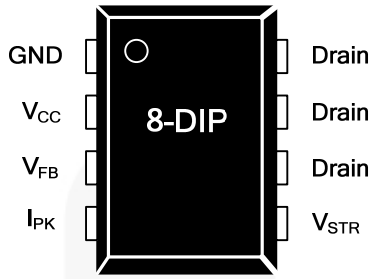

Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. SenseFET source terminal on the primary side and internal control ground.
2	V_{CC}	**Positive Supply Voltage Input**. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V_{STR}) via an internal switch during startup (*see Figure 2*). Once V_{CC} reaches the UVLO upper threshold (12V), the internal startup switch opens and device power is supplied via the auxiliary transformer winding.
3	V_{FB}	**Feedback Voltage**. The non-inverting input to the PWM comparator, it has a 0.4mA current source connected internally, while a capacitor and opto-coupler are typically connected externally. There is a delay while charging external capacitor C_{FB} from 2.4V to 6V using an internal 5μA current source. This delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
4	I_{PK}	**Peak Current Limit**. Adjusts the peak current limit of the SenseFET. The feedback 0.4mA current source is diverted to the parallel combination of an internal 6kΩ resistor and any external resistor to GND on this pin to determine the peak current limit.
5	V_{STR}	**Startup**. Connected to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the V_{CC} pin and ground. Once V_{CC} reaches 12V, the internal switch is opened.
6, 7, 8	Drain	**Drain**. Designed to connect directly to the primary lead of the transformer and capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_J = 25°C, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage	-0.3	650.0	V
V_{DS}	Drain Pin Voltage	-0.3	650.0	V
V_{CC}	Supply Voltage		26	V
V_{FB}	Feedback Voltage Range	-0.3	12.0	V
I_D	Continuous Drain Current		0.7	A
I_{DM}	Drain Current Pulsed[4]		2.8	A
E_{AS}	Single Pulsed Avalanche Energy[5]		15	mJ
P_D	Total Power Dissipation		1.5	W
T_J	Operating Junction Temperature	Internally Limited		°C
T_A	Operating Ambient Temperature	-40	+105	°C
T_{STG}	Storage Temperature	-55	+150	°C
ESD	Human Body Model, JESD22-A114[6]	5		KV
	Charged Device Model, JESD22-C101[6]	2		
Θ_{JA}	Junction-to-Ambient Thermal Resistance[7,8]		80	°C/W
Θ_{JC}	Junction-to-Case Thermal Resistance[7,9]		19	°C/W
Θ_{JT}	Junction-to-Top Thermal Resistance[7,10]		33.7	°C/W

Notes:

4. Repetitive rating: pulse width limited by maximum junction temperature.
5. L=30mH, starting T_J=25°C.
6. Meets JEDEC standards JESD 22-A114 and JESD 22-C101.
7. All items are tested with the standards JESD 51-2 and JESD 51-10.
8. Θ_{JA} free-standing, with no heat-sink, under natural convection.
9. Θ_{JC} junction-to-lead thermal characteristics under Θ_{JA} test condition. T_C is measured on the source #7 pin closed to plastic interface for Θ_{JA} thermo-couple mounted on soldering.
10. Θ_{JT} junction-to-top of thermal characteristic under Θ_{JA} test condition. T_t is measured on top of package. Thermo-couple is mounted in epoxy glue.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
SenseFET Section							
BV_{DSS}	Drain-Source Breakdown Voltage		V_{CC} = 0V, I_D = 250μA	650			V
I_{DSS}	Zero Gate Voltage Drain Current		V_{DS} = 650V, V_{GS} = 0V			250	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance		V_{GS} = 10V, V_{GS} = 0V, T_C = 25°C		11.5	18.0	Ω
C_{ISS}	Input Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		137		pF
C_{OSS}	Output Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		15.7		pF
C_{RSS}	Reverse Transfer Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		2.9		pF
$t_{d(ON)}$	Turn-On Delay		V_{DD} = 350V, I_D = 0.7A		8.6		ns
t_r	Rise Time		V_{DD} = 350V, I_D = 0.7A		9.7		ns
$t_{d(OFF)}$	Turn-Off Delay		V_{DD} = 350V, I_D = 0.7A		23.6		ns
t_f	Fall Time		V_{DD} = 350V, I_D = 0.7A		49.2		ns
Control Section							
f_{OSC}	Switching Frequency		V_{DS} = 650V, V_{GS} = 0V	90	100	110	KHz
Δf_{OSC}	Switching Frequency Variation		V_{GS} = 10V, V_{GS} = 0V, T_C = 125°C		±5	±10	%
f_{FM}	Frequency Modulation				±3		KHz
D_{MAX}	Maximum Duty Cycle		V_{FB} = 4V	71	77	83	%
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0V	0	0	0	%
V_{START}	UVLO Threshold Voltage			11	12	13	V
V_{STOP}			After Turn-On	7	8	9	V
I_{FB}	Feedback Source Current		V_{FB} = 0V	320	400	480	μA
$t_{S/S}$	Internal Soft-Start Time		V_{FB} = 4V	15	20	25	ms
Burst Mode Section							
V_{BURH}	Burst Mode Voltage		T_J = 25°C	0.56	0.70	0.84	V
V_{BURL}				0.37	0.50	0.63	V
$V_{BUR(HYS)}$					200		mV
Protection Section							
I_{LIM}	Peak Current Limit		T_J = 25°C, di/dt = 300mA/μs	0.62	0.70	0.84	A
t_{CLD}	Current Limit Delay Time(11)			200			ns
V_{SD}	Shutdown Feedback Voltage		V_{CC} = 15V	5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 5V	3.5	5.0	6.5	μA
V_{OVP}	Over-Voltage Protection Threshold		V_{FB} = 2V	22.5	24.0	25.5	V
t_{OSP}	Output-Short Protection(11)	Threshold Time	T_J = 25°C OSP Triggered When t_{ON}<t_{OSP}, V_{FB}>V_{OSP} and Lasts Longer than t_{OSP_FB}		1.00	1.35	μs
V_{OSP}		Threshold Feedback Voltage		1.44	1.60		V
t_{OSP_FB}		Feedback Blanking Time		2.0	2.5		μs
V_{AOCP}	AOCP Voltage(11)		T_J = 25°C	0.85	1.00	1.15	V
TSD	Thermal Shutdown(11)	Shutdown Temperature		125	137	150	°C
HYS_{TSD}		Hysteresis			60		°C
t_{LEB}	Leading-Edge Blanking Time(11)			300			ns

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Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Total Device Section						
I_{OP1}	Operating Supply Current(11) (While Switching)	V_{CC} = 14V, V_{FB} > V_{BURH}		2.5	3.5	mA
I_{OP2}	Operating Supply Current (Control Part Only)	V_{CC} = 14V, V_{FB} < V_{BURL}		1.8	2.5	mA
I_{CH}	Startup Charging Current	V_{CC} = 0V	0.9	1.1	1.3	mA
V_{STR}	Minimum V_{STR} Supply Voltage	V_{CC} = V_{FB} = 0V, V_{STR} Increase	35			V

Note:

11. Though guaranteed by design, it is not 100% tested in production.