

# FSFR-US Series — Fairchild Power Switch (FPS™) for Half-Bridge Resonant Converters

## Features

- Variable Frequency Control with 50% Duty Cycle for Half-Bridge Resonant Converter Topology
- High Efficiency through Zero Voltage Switching (ZVS)
- Internal UniFET™s with Fast-Recovery Type Body Diode
- Fixed Dead Time (350ns) Optimized for MOSFETs
- Up to 300kHz Operating Frequency
- Auto-Restart Operation for All Protections with An External LV<sub>CC</sub>
- Protection Functions: Over-Voltage Protection (OVP), Over-Current Protection (OCP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD)

## Applications

- PDP and LCD TVs
- Desktop PCs and Servers
- Adapters
- Telecom Power Supplies

## Description

The FSFR-US series are a highly integrated power switches designed for high-efficiency half-bridge resonant converters. Offering everything necessary to build a reliable and robust resonant converter, the FSFR-US series simplifies designs and improves productivity, while improving performance. The FSFR-US series combines power MOSFETs with fast-recovery type body diodes, a high-side gate-drive circuit, an accurate current controlled oscillator, frequency limit circuit, soft-start, and built-in protection functions. The high-side gate-drive circuit has a common-mode noise cancellation capability, which guarantees stable operation with excellent noise immunity. The fast-recovery body diode of the MOSFETs improves reliability against abnormal operation conditions, while minimizing the effect of the reverse recovery. Using the zero-voltage-switching (ZVS) technique dramatically reduces the switching losses and efficiency is significantly improved. The ZVS also reduces the switching noise noticeably, which allows a small-sized Electromagnetic Interference (EMI) filter.

The FSFR-US series can be applied to various resonant converter topologies such as series resonant, parallel resonant, and LLC resonant converters.

## Related Resources

[AN4151 — Half-bridge LLC Resonant Converter Design using FSFR-Series Fairchild Power Switch \(FPS™\)](#)

## Ordering Information

Part Number	Package	Operating Junction Temperature	R <sub>DS(ON_MAX)</sub>	Maximum Output Power without Heatsink (V <sub>IN</sub> =350~400V) <sup>(1,2)</sup>	Maximum Output Power with Heatsink (V <sub>IN</sub> =350~400V) <sup>(1,2)</sup>
FSFR2100US	9-SIP	-40 to +130°C	0.51Ω	180W	400W
FSFR1800US			0.95Ω	120W	260W
FSFR1700US			1.25Ω	100W	200W
FSFR2100USL	9-SIP L-Forming		0.51Ω	180W	400W
FSFR1800USL			0.95Ω	120W	260W
FSFR1700USL			1.25Ω	100W	200W

### Notes:

1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open-frame design at 50°C ambient.

## Pin Configuration

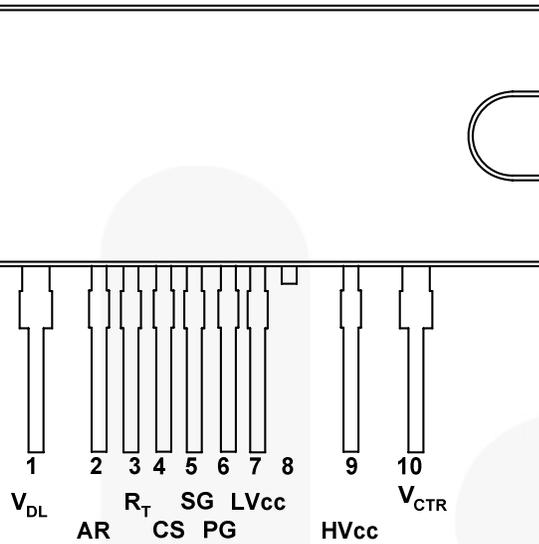


Figure 3. Package Diagram

## Pin Definitions

Pin #	Name	Description
1	$V_{DL}$	This is the drain of the high-side MOSFET, typically connected to the input DC link voltage.
2	AR	This pin is for discharging the external soft-start capacitor when any protections are triggered. When the voltage of this pin drops to 0.2, all protections are reset and the controller starts to operate again.
3	$R_T$	This pin programs the switching frequency. Typically, an opto-coupler is connected to control the switching frequency for the output voltage regulation.
4	CS	This pin senses the current flowing through the low-side MOSFET. Typically, negative voltage is applied on this pin.
5	SG	This pin is the control ground.
6	PG	This pin is the power ground. This pin is connected to the source of the low-side MOSFET.
7	$LV_{CC}$	This pin is the supply voltage of the control IC.
8	NC	No connection.
9	$HV_{CC}$	This is the supply voltage of the high-side gate-drive circuit IC.
10	$V_{CTR}$	This is the drain of the low-side MOSFET. Typically, a transformer is connected to this pin.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A=25^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
$V_{DS}$	Maximum Drain-to-Source Voltage ( $V_{DL}-V_{CTR}$ and $V_{CTR}-PG$ )	500		V
$LV_{CC}$	Low-Side Supply Voltage	-0.3	25.0	V
$HV_{CC}$ to $V_{CTR}$	High-Side $V_{CC}$ Pin to Low-Side Drain Voltage	-0.3	25.0	V
$HV_{CC}$	High-Side Floating Supply Voltage	-0.3	525.0	V
$V_{AR}$	Auto-Restart Pin Input Voltage	-0.3	$LV_{CC}$	V
$V_{CS}$	Current Sense (CS) Pin Input Voltage	-5.0	1.0	V
$V_{RT}$	$R_T$ Pin Input Voltage	-0.3	5.0	V
$dV_{CTR}/dt$	Allowable Low-Side MOSFET Drain Voltage Slew Rate		50	V/ns
$P_D$	Total Power Dissipation <sup>(3)</sup>	FSFR2100US/L	12.0	W
		FSFR1800US/L	11.7	
		FSFR1700US/L	11.6	
$T_J$	Maximum Junction Temperature <sup>(4)</sup>		+150	$^{\circ}\text{C}$
	Recommended Operating Junction Temperature <sup>(4)</sup>	-40	+130	
$T_{STG}$	Storage Temperature Range	-55	+150	$^{\circ}\text{C}$

**Notes:**

3. Per MOSFET when both MOSFETs are conducting.
4. The maximum value of the recommended operating junction temperature is limited by thermal shutdown.

### Absolute Maximum Ratings (Continued)

Symbol	Parameter		Min.	Max.	Unit
<b>MOSFET Section</b>					
V <sub>DGR</sub>	Drain Gate Voltage (R <sub>GS</sub> =1MΩ)		500		V
V <sub>GS</sub>	Gate Source (GND) Voltage			±30	V
I <sub>DM</sub>	Drain Current Pulsed <sup>(5)</sup>	FSFR2100US/L		32	A
		FSFR1800US/L		23	
		FSFR1700US/L		20	
I <sub>D</sub>	Continuous Drain Current	FSFR2100US/L	T <sub>C</sub> =25°C	10.5	A
			T <sub>C</sub> =100°C	6.5	
		FSFR1800US/L	T <sub>C</sub> =25°C	7.0	
			T <sub>C</sub> =100°C	4.5	
		FSFR1700US/L	T <sub>C</sub> =25°C	6.0	
			T <sub>C</sub> =100°C	3.9	
<b>Package Section</b>					
Torque	Recommended Screw Torque		5~7		kgf·cm

**Notes:**

5. Pulse width is limited by maximum junction temperature.

### Thermal Impedance

T<sub>A</sub>=25°C unless otherwise specified.

Symbol	Parameter		Value	Unit
θ <sub>JC</sub>	Junction-to-Case Center Thermal Impedance (Both MOSFETs Conducting)	FSFR2100US/L	10.44	°C/W
		FSFR1800US/L	10.68	
		FSFR1700US/L	10.79	

## Electrical Characteristics

T<sub>A</sub>=25°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Specifications			Unit
			Min.	Typ.	Max.	
<b>MOSFET Section</b>						
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	I <sub>D</sub> =200μA, T <sub>A</sub> =25°C	500			V
		I <sub>D</sub> =200μA, T <sub>A</sub> =125°C		540		
R <sub>DS(ON)</sub>	On-State Resistance	FSFR2100US/L V <sub>GS</sub> =10V, I <sub>D</sub> =6.0A		0.41	0.51	Ω
		FSFR1800US/L V <sub>GS</sub> =10V, I <sub>D</sub> =3.0A		0.77	0.95	
		FSFR1700US/L V <sub>GS</sub> =10V, I <sub>D</sub> =2.0A		1.00	1.25	
t <sub>rr</sub>	Body Diode Reverse Recovery Time <sup>(6)</sup>	FSFR2100US/L V <sub>GS</sub> =0V, I <sub>Diode</sub> =12.0A, dI <sub>Diode</sub> /dt=100A/μs		120		ns
		FSFR1800US/L V <sub>GS</sub> =0V, I <sub>Diode</sub> =7.0A, dI <sub>Diode</sub> /dt=100A/μs		160		
		FSFR1700US/L V <sub>GS</sub> =0V, I <sub>Diode</sub> =6.0A, dI <sub>Diode</sub> /dt=100A/μs		160		
<b>Supply Section</b>						
I <sub>LK</sub>	Offset Supply Leakage Current	H-V <sub>CC</sub> =V <sub>CTR</sub> =500V			50	μA
I <sub>QHVCC</sub>	Quiescent HV <sub>CC</sub> Supply Current	(HV <sub>CC</sub> UV+) - 0.1V		50	120	μA
I <sub>QLVCC</sub>	Quiescent LV <sub>CC</sub> Supply Current	(LV <sub>CC</sub> UV+) - 0.1V		100	200	μA
I <sub>oHVCC</sub>	Operating HV <sub>CC</sub> Supply Current (RMS Value)	f <sub>OSC</sub> =100KHz		6	9	mA
		No Switching		100	200	μA
I <sub>oLVCC</sub>	Operating LV <sub>CC</sub> Supply Current (RMS Value)	f <sub>OSC</sub> =100KHz		7	11	mA
		No Switching		2	4	mA
<b>UVLO Section</b>						
LV <sub>CC</sub> UV+	LV <sub>CC</sub> Supply Under-Voltage Positive Going Threshold (LV <sub>CC</sub> Start)		11.2	12.5	13.8	V
LV <sub>CC</sub> UV-	LV <sub>CC</sub> Supply Under-Voltage Negative Going Threshold (LV <sub>CC</sub> Stop)		8.90	10.0	11.1	V
LV <sub>CC</sub> UVH	LV <sub>CC</sub> Supply Under-Voltage Hysteresis			2.50		V
HV <sub>CC</sub> UV+	HV <sub>CC</sub> Supply Under-Voltage Positive Going Threshold (HV <sub>CC</sub> Start)		8.2	9.2	10.2	V
HV <sub>CC</sub> UV-	HV <sub>CC</sub> Supply Under-Voltage Negative Going Threshold (HV <sub>CC</sub> Stop)		7.8	8.7	9.6	V
HV <sub>CC</sub> UVH	HV <sub>CC</sub> Supply Under-Voltage Hysteresis			0.5		V

**Electrical Characteristics** (Continued)

 $T_A=25^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Test Conditions	Specifications			Unit
			Min	Typ	Max	
<b>Oscillator &amp; Feedback Section</b>						
$V_{RT}$	V-I Converter Threshold Voltage	$R_T=5.2\text{K}\Omega$	1.5	2.0	2.5	V
$f_{OSC}$	Output Oscillation Frequency		94	100	106	KHz
DC	Output Duty Cycle		48	50	52	%
$f_{SS}$	Internal Soft-Start Initial Frequency	$f_{SS}=f_{OSC}+40\text{kHz}$ , $R_T=5.2\text{K}\Omega$		140		KHz
$t_{SS}$	Internal Soft-Start Time		2	3	4	ms
<b>Protection Section</b>						
$V_{C_{SS}H}$	Beginning Voltage to Discharge $C_{SS}$		0.9	1.0	1.1	V
$V_{C_{SS}L}$	Beginning Voltage to Charge $C_{SS}$ and Restart		0.16	0.20	0.24	V
$V_{OVP}$	LV <sub>CC</sub> Over-Voltage Protection	$L-V_{CC} > 21\text{V}$	21	23	25	V
$V_{AOCP}$	AOCP Threshold Voltage	$\Delta V/\Delta t=-0.1\text{V}/\mu\text{s}$	-1.0	-0.9	-0.8	V
$t_{BAO}$	AOCP Blanking Time <sup>(6)</sup>	$V_{CS} < V_{AOCP}$ ; $\Delta V/\Delta t=-0.1\text{V}/\mu\text{s}$		50		ns
$V_{OCP}$	OCP Threshold Voltage	$V/\Delta t=-1\text{V}/\mu\text{s}$	-0.64	-0.58	-0.52	V
$t_{BO}$	OCP Blanking Time <sup>(6)</sup>	$V_{CS} < V_{OCP}$ ; $\Delta V/\Delta t=-1\text{V}/\mu\text{s}$	1.0	1.5	2.0	$\mu\text{s}$
$t_{DA}$	Delay Time (Low Side) Detecting from $V_{AOCP}$ to Switch Off <sup>(6)</sup>	$\Delta V/\Delta t=-1\text{V}/\mu\text{s}$		250	400	ns
$T_{SD}$	Thermal Shutdown Temperature <sup>(6)</sup>		120	135	150	$^{\circ}\text{C}$
<b>Dead-Time Control Section</b>						
$D_T$	Dead Time <sup>(7)</sup>			350		ns

**Notes:**

6. This parameter, although guaranteed, is not tested in production.
7. These parameters, although guaranteed, are tested only in EDS (wafer test) process.