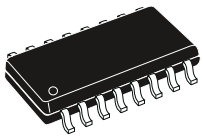
L6699

Enhanced high voltage resonant controller

Datasheet – production data

Features

- Symmetrical duty cycle, variable frequency control of resonant half bridge
- Self-adjusting adaptive deadtime
- High-accuracy oscillator
- 2-level OCP: frequency-shift and immediate shutdown
- Interface with PFC controller
- Anti-capacitive-mode protection
- Burst-mode operation at light load
- Input for brownout protection or power-on/off sequencing
- “Safe-start” procedure prevents hard switching at startup
- 600 V rail compatible high-side gate driver with integrated bootstrap diode and high dv/dt immunity
- -300/800 mA high-side and low-side gate drivers with UVLO pull-down
- SO16N package



SO16N

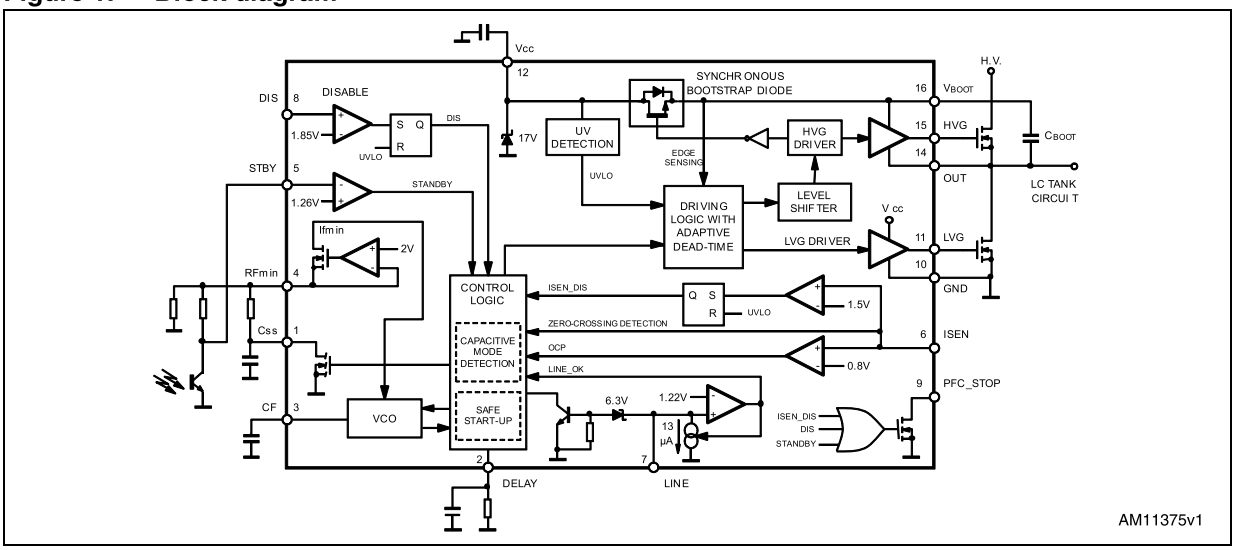
Applications

- SMPS for LCD TVs, desktop and AIO PCs, servers, Telecom power
- AC-DC adapter, open frame SMPS

Table 1. Device summary

Order codes	Package	Packing
L6699D	SO16N	Tube
L6699DTR		Tape and reel

Figure 1. Block diagram



4 Pin connections

Figure 2. Pin connections (top view)

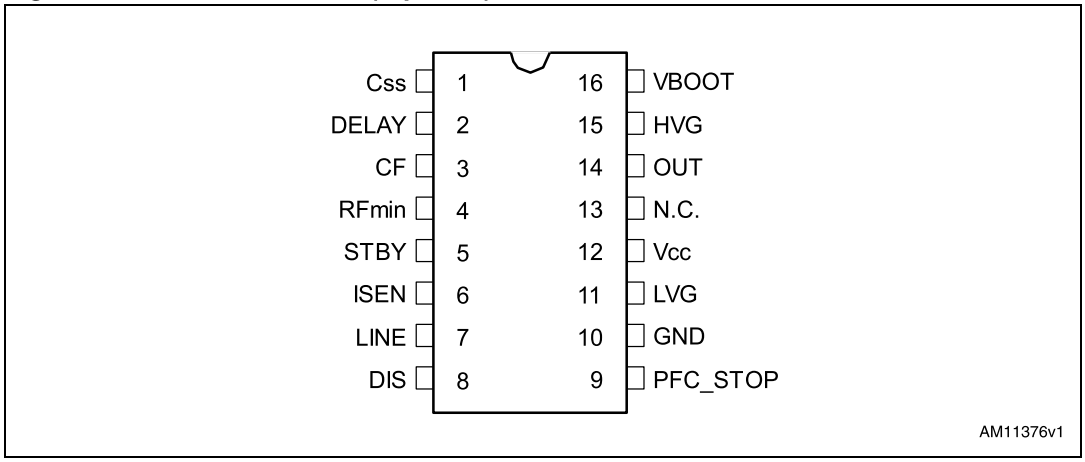


Table 4. Pin functions

N.	Name	Function
1	C_{SS}	Soft-start. This pin connects an external capacitor to GND and a resistor to RF_{min} (pin 4) that set both the initial oscillator frequency and the time constant for the frequency shift that occurs as the chip starts up (soft-start). An internal switch discharges this capacitor every time the chip turns off (V_{CC} < UVLO, LINE < 1.25 V, DIS > 1.85 V, ISEN > 1.5 V, DELAY > 2 V) to make sure it is soft-started next. Additionally the switch is activated when the voltage on the current sense pin (ISEN) exceeds 0.8 V or when the converter is working too close to, or in, the capacitive-mode operation.
2	DELAY	Delayed shutdown upon overcurrent. A capacitor and a resistor are connected from this pin to GND to set both the maximum duration of an overcurrent condition before the IC stops switching and the delay after which the IC restarts switching. Every time the voltage on the ISEN pin exceeds 0.8 V the capacitor is charged by 350 µA current pulses and is slowly discharged by the external resistor. If the voltage on the DELAY pin reaches 2 V, the soft-start capacitor is completely discharged so that the switching frequency is pushed to its maximum value and the 350 µA current source is kept always on. As the voltage on the DELAY pin exceeds 3.5 V the IC stops switching and the internal generator is turned off, so that the voltage on the pin decays because of the external resistor. The IC is soft-restarted as the voltage drops below 0.3 V. In this way, under short-circuit conditions, the converter works intermittently with very low input average power. If the voltage on the ISEN pin exceeds 1.5 V, the L6699 is immediately stopped and the 350 µA current source is kept on until the voltage on the DELAY pin reaches 3.5 V. Then, the generator is turned off and the voltage on the pin decays because of the external resistor. Also in this case the IC is soft-restarted as the voltage drops below 0.3 V.
3	CF	Timing capacitor. A capacitor connected from this pin to GND is charged and discharged by internal current generators programmed by the external network connected to pin 4 (RF_{min}) and determines the switching frequency of the converter.

Table 4. Pin functions (continued)

N.	Name	Function
4	RF_{min}	Minimum oscillator frequency setting. This pin provides an accurate 2 V reference, and a resistor connected from this pin to GND defines a current that is used to set the minimum oscillator frequency. To close the feedback loop that regulates the converter output voltage by modulating the oscillator frequency, the phototransistor of an optocoupler is connected to this pin through a resistor. The value of this resistor sets the maximum operating frequency. Initial operating frequency should be set below 300 kHz; it is recommended not to exceed such limit. An R-C series connected from this pin to GND sets frequency shift at startup to prevent excessive energy inrush (soft-start).
5	STBY	Burst-mode operation threshold. The pin senses some voltage related to the feedback control, which is compared to an internal reference (1.26 V). If the voltage on the pin is lower than the reference, the IC enters an idle state and its quiescent current is reduced. The chip restarts switching as the voltage exceeds the reference by 30 mV. Soft-start is not invoked. This function realizes burst-mode operation when the load falls below a level that can be programmed by properly choosing the resistor connecting the optocoupler to the RF_{min} pin (see *Figure 1: Block diagram*). Tie the pin to RF_{min} if burst-mode is not used.
6	ISEN	Current sense input. The pin senses the instantaneous primary current though a sense resistor or a capacitive divider for lossless sensing. If the voltage exceeds a 0.8 V threshold the soft-start capacitor connected to pin 1 is internally discharged: the frequency increases and so limits the power throughput. Under output short-circuit, this normally results in a nearly constant peak primary current. This condition is allowed for a maximum time set at pin 2. If the current keeps on building up despite this frequency increase, a second comparator referenced to 1.5 V disables switching immediately and activates a restart delay procedure (see DELAY pin description for more information). This pin is used also for capacitive-mode operation detection and for hard-switching prevention at startup. Do not short the pin to ground; this would prevent the device from operating correctly.
7	LINE	Line sensing input. The pin is to be connected to the high voltage input bus with a resistor divider to perform either AC or DC (in systems with PFC) brownout protection. A voltage below 1.25 V shuts down the IC, lowers its consumption and discharges the soft-start capacitor. IC operation is enabled as the voltage exceeds 1.25 V. The comparator is provided with current hysteresis: an internal 13 µA current generator is ON as long as the voltage applied at the pin is below 1.25 V, and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND to reduce noise pick-up. The voltage on the pin is top-limited by an internal Zener. Tie the pin to V_{CC} with a =100 kΩ resistor if not used.
8	DIS	Latched device shutdown. Internally, the pin connects a comparator that, when the voltage on the pin exceeds 1.85 V, shuts the IC down and brings its consumption almost to a “before startup” level. The information is latched and it is necessary to recycle the supply voltage of the IC to enable it to restart: the latch is removed as the voltage on the V_{CC} pin goes below the UVLO threshold. Tie the pin to GND if the function is not used.
9	PFC_STOP	Open-drain ON/OFF control of PFC controller. This pin, normally open, is intended for stopping the PFC controller, for protection purposes or during burst-mode operation. It goes low when the IC is shut down by DIS > 1.85 V, ISEN > 1.5 V and STBY < 1.25 V. The pin is pulled low also when capacitive mode operation is detected and when the voltage on the DELAY pin exceeds 2 V. In this latter case it goes back open as the voltage falls below 0.3 V. During UVLO, it is open. Leave the pin unconnected if not used.

Table 4. Pin functions (continued)

N.	Name	Function
10	GND	Chip ground. Current return for both the low-side gate-drive current and the bias current of the IC. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
11	LVG	Low-side gate-drive output. The driver is capable of 0.3 A min. source and 0.8 A min. sink peak current to drive the lower MOSFET of the half bridge leg. The pin is actively pulled to GND during UVLO.
12	V_{CC}	Supply voltage of both the signal part of the IC and the low-side gate driver. Sometimes a small bypass capacitor (0.1 µF typ.) to GND may be useful to obtain a clean bias voltage for the signal part of the IC.
13	N.C.	High voltage spacer. The pin is not internally connected to isolate the high voltage pin and ease compliance with safety regulations (creepage distance) on the PCB.
14	OUT	High-side gate-drive floating ground. Current return for the high-side gate-drive current. Lay out the connection of this pin carefully to avoid too large spikes below ground.
15	HVG	High-side floating gate-drive output. The driver is capable of 0.3 A min. source and 0.8 A min. sink peak current to drive the upper MOSFET of the half bridge leg. A resistor internally connected to pin 14 (OUT) ensures that the pin is not floating during UVLO.
16	V_{BOOT}	High-side gate-drive floating supply voltage. The bootstrap capacitor connected between this pin and pin 14 (OUT) is fed by an internal synchronous bootstrap diode driven in-phase with the low-side gate-drive. This patented structure replaces the normally used external diode.

Figure 3. Typical system block diagram