

**600V High and Low Side Driver**
**PRODUCT SUMMARY**

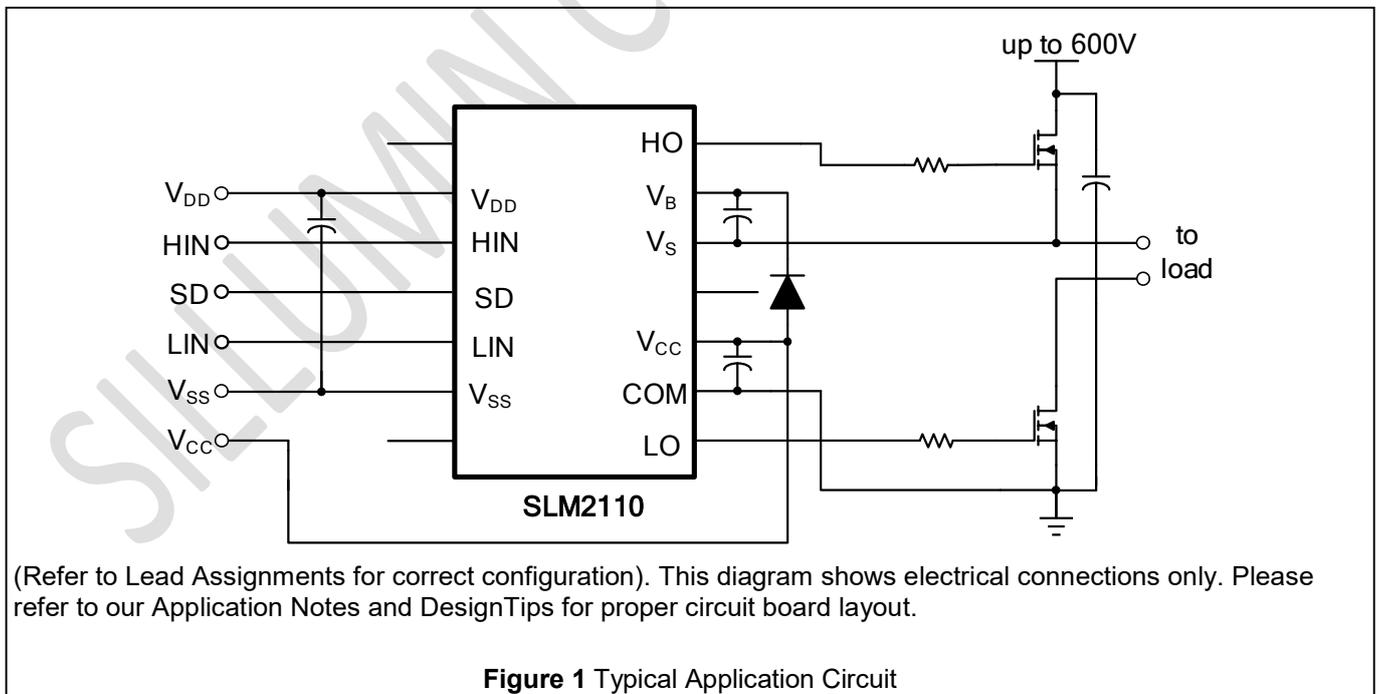
- $V_{\text{OFFSET}}$  600 V max.
- $I_{\text{O}+/-}$  2.5 A / 2.5 A
- $V_{\text{OUT}}$  10 V - 20 V
- $t_{\text{on/off}}$  (typ.) 130 ns/120 ns
- **Delay Matching (typ.)** 10 ns

**GENERAL DESCRIPTION**

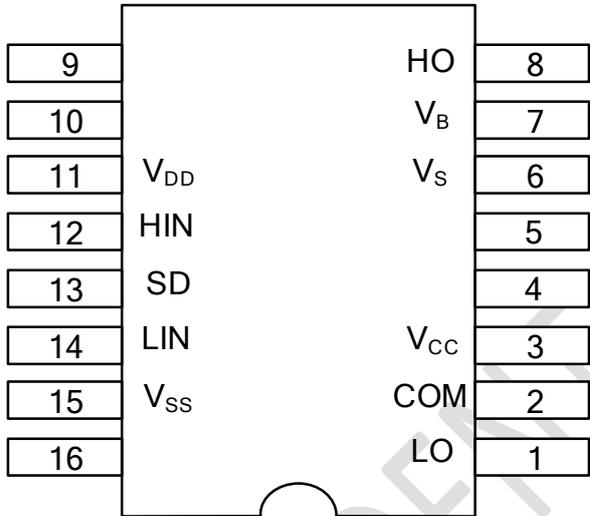
The SLM2110 is a high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

**FEATURES**

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V logic compatible
- Logic and power ground +/- 5V offset
- Cross-conduction prevention logic
- CMOS Schmitt-triggered inputs with pull-down
- Cycle-by-cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant
- SOIC-16 (WB) package

**TYPICAL APPLICATION CIRCUIT**


**PIN CONFIGURATION**

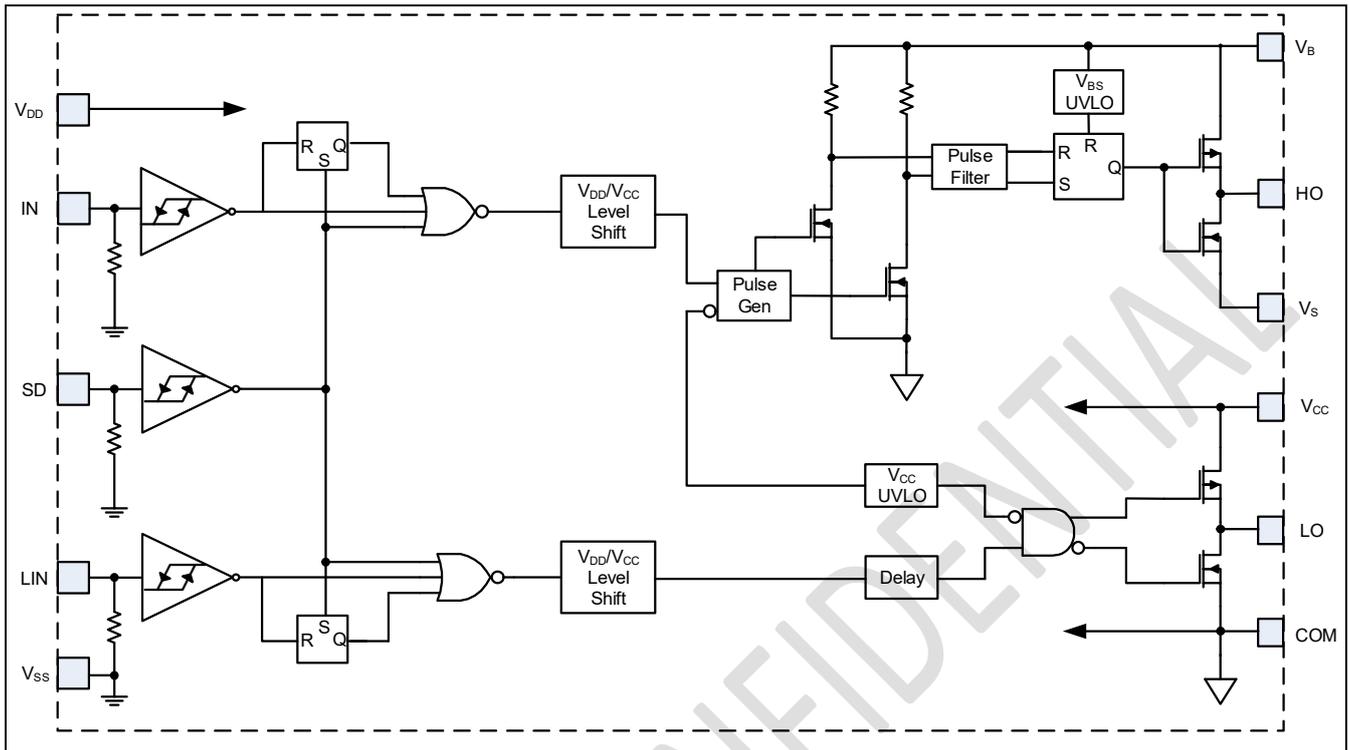
Package	Pin Configuration (Top View)
SOIC-16 (WB)	

**PIN DESCRIPTION**

No.	Pin	Description
1	LO	Low-side gate drive output
2	COM	Low-side return
3	V <sub>CC</sub>	Low-side supply
4	NC	No connection
5	NC	No connection
6	V <sub>s</sub>	High-side floating supply return
7	V <sub>B</sub>	High-side floating supply
8	HO	High-side gate drive output
9	NC	No connection
10	NC	No connection
11	V <sub>DD</sub>	Logic supply
12	HIN	Logic input for high-side gate driver output (HO), in phase
13	SD	Logic input for shutdown
14	LIN	Logic input for low-side gate driver output (LO), in phase
15	V <sub>SS</sub>	Logic ground
16	NC	No connection

**ORDERING INFORMATION**
**Industrial Range: -40°C to +125°C**

Order Part No.	Package	QTY
SLM2110CG	SOIC16 (WB), Pb-Free	1500/Reel

**FUNCTIONAL BLOCK DIAGRAM**

**SLM2110**

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Definition	Min.	Max.	Units	
$V_B$	High-side floating absolute voltage	-0.3	625	V	
$V_S$	High-side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$		
$V_{HO}$	High-side floating output voltage	$V_S - 0.3$	$V_B + 0.3$		
$V_{CC}$	Low-side supply voltage	-0.3	25		
$V_{DD}$	Logic supply voltage	-0.3	$V_{SS} + 20$		
$V_{SS}$	Logic supply offset voltage	$V_{CC} - 20$	$V_{CC} + 0.3$		
$V_{LO}$	Low-side output voltage	-0.3	$V_{CC} + 0.3$		
$V_{IN}$	Logic input voltage (HIN, LIN, & SD)	$V_{SS} - 0.3$	$V_{DD} + 0.3$		
$dV_S/dt$	Allowable offset supply voltage transient	---	50	V/ns	
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	SOIC-16 (WB)	---	1.25	W
$R_{thJA}$	Thermal resistance, junction to ambient	SOIC-16 (WB)	---	100	$^\circ\text{C}/\text{W}$
$T_J$	Junction temperature	---	150	$^\circ\text{C}$	
$T_S$	Storage temperature	-55	150		
$T_L$	Lead temperature (soldering, 10 seconds)	---	300		

**Note:**

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Definition	Min.	Max.	Units
$V_B$	High-side floating absolute voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	High-side floating supply offset voltage	Note 1	600	
$V_{HO}$	High-side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low-side supply voltage	10	20	
$V_{DD}$	Logic supply voltage	$V_{SS} + 3$	$V_{SS} + 20$	
$V_{SS}$	Logic supply offset voltage	-5	5	
$V_{LO}$	Low-side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage (HIN, LIN, & SD)	$V_{SS}$	$V_{DD}$	
$T_A$	Ambient temperature	- 40	125	$^\circ\text{C}$

**Note:**

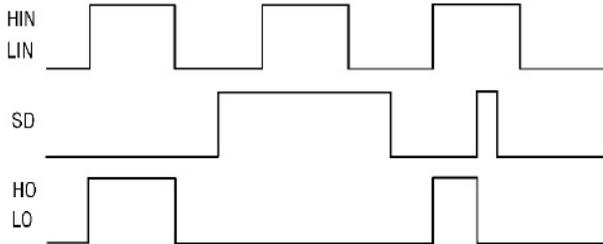
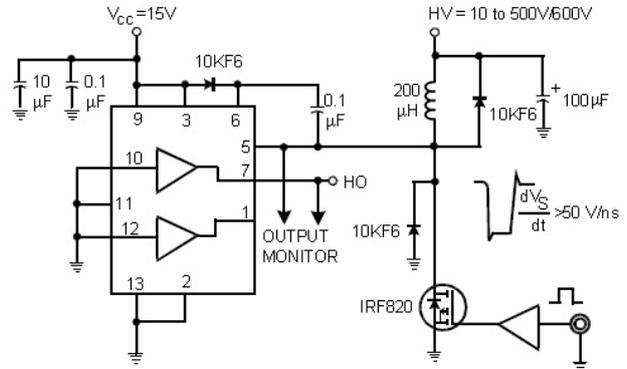
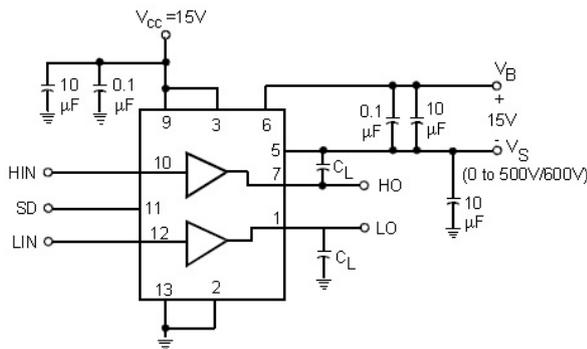
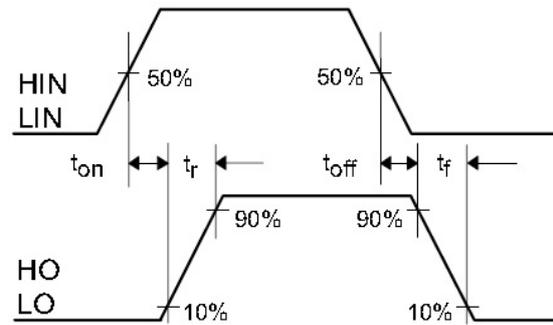
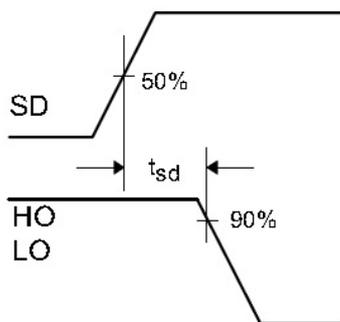
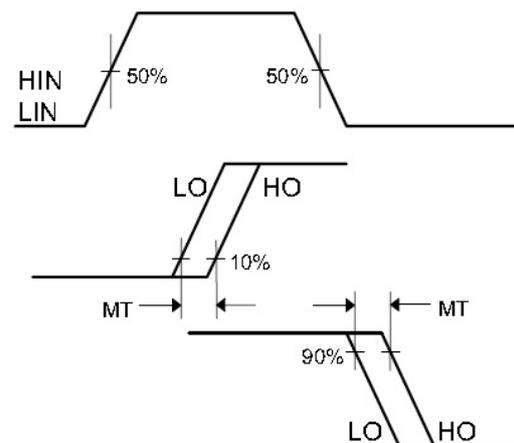
The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at a 15 V differential.

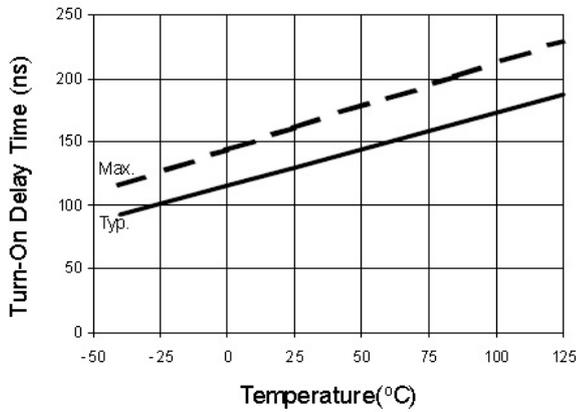
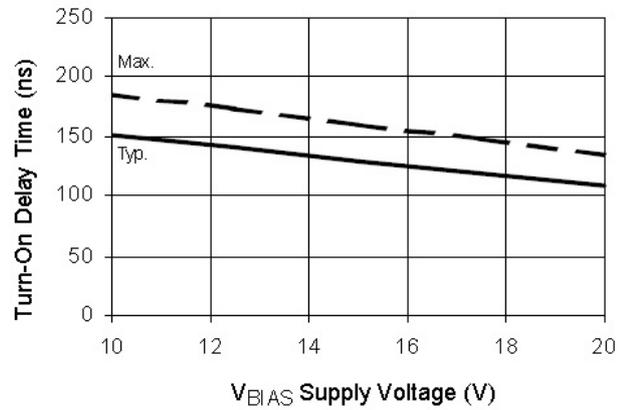
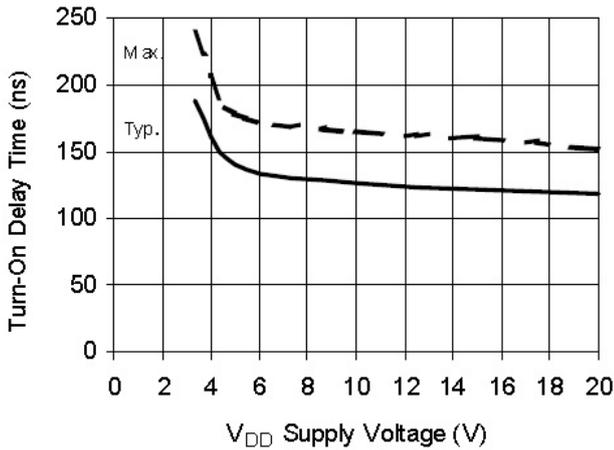
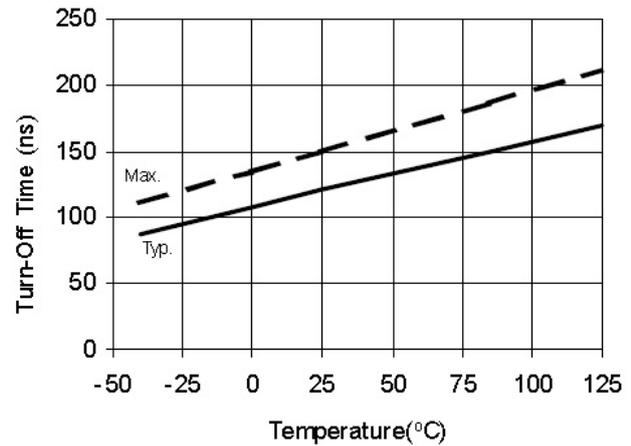
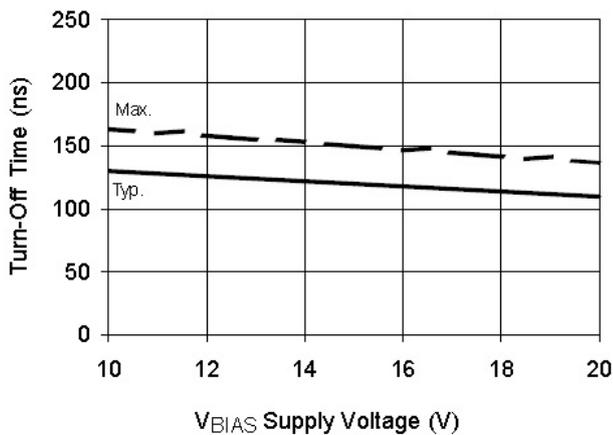
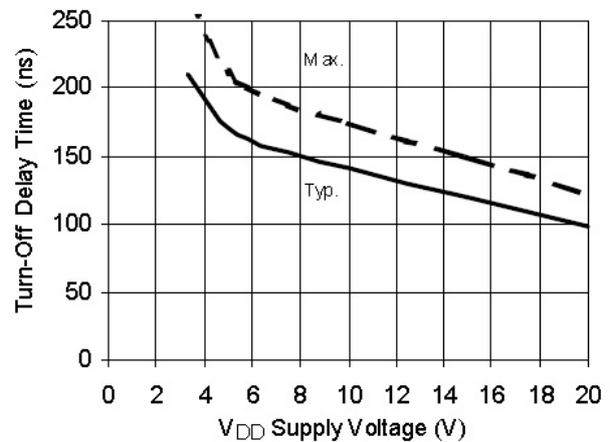
**DYNAMIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15\text{ V}$ ,  $C_L = 1000\text{ pF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

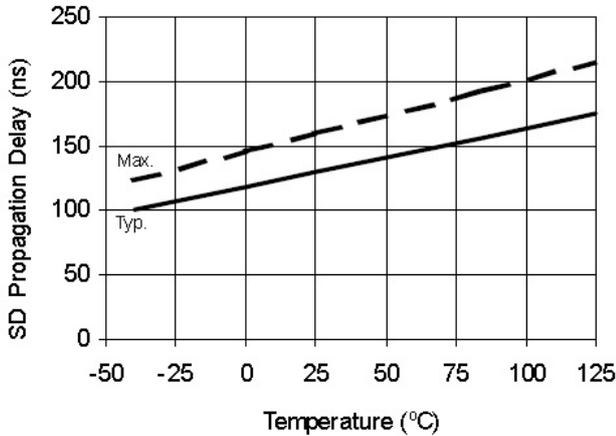
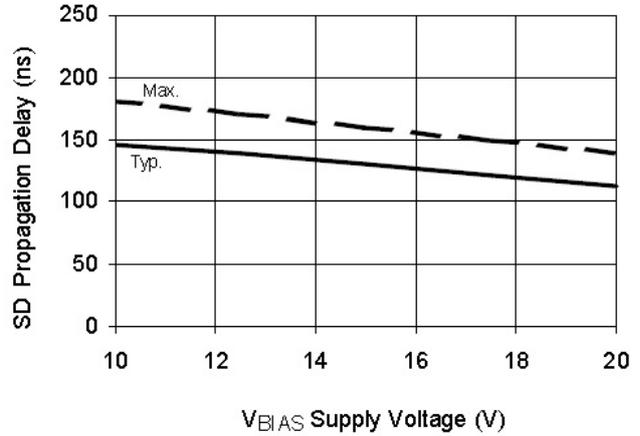
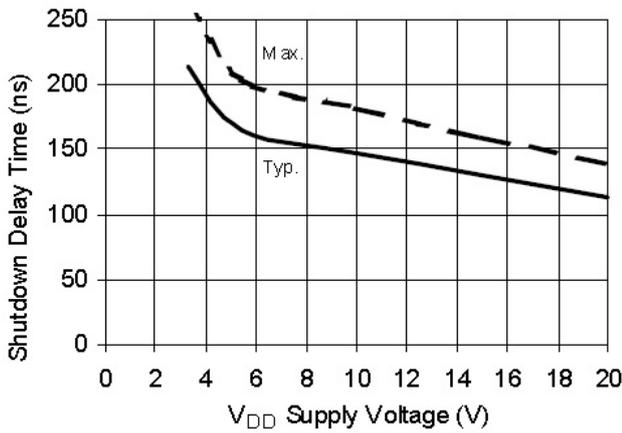
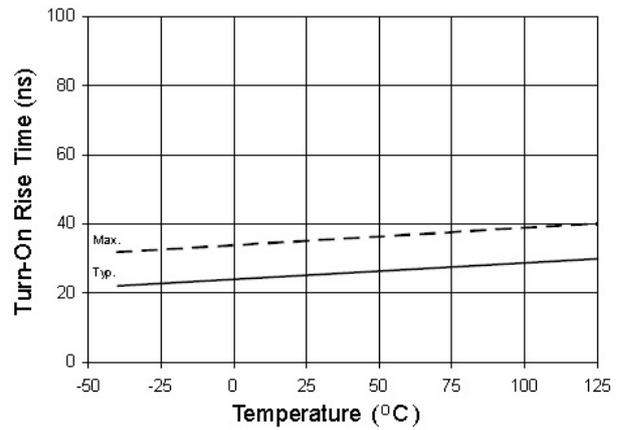
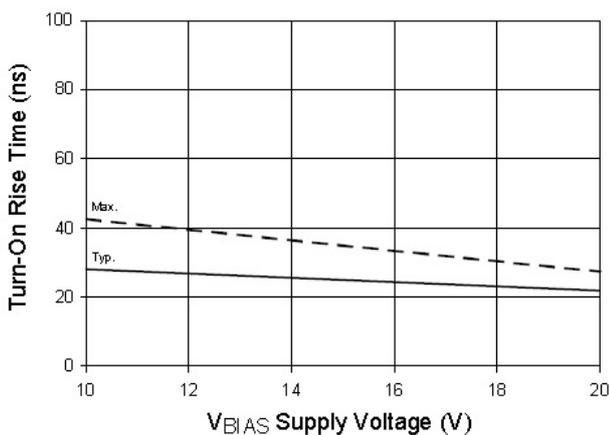
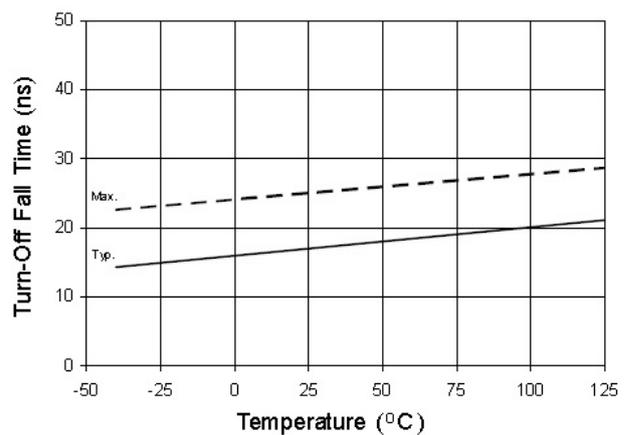
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on propagation delay	$V_S = 0\text{ V}$	---	130	160	ns
$t_{off}$	Turn-off propagation delay	$V_S = 600\text{ V}$	---	120	150	
$t_{sd}$	Shutdown propagation delay	$V_S = 600\text{ V}$	---	130	160	
$t_r$	Turn-on rise time		---	25	35	
$t_f$	Turn-off fall time		---	17	25	
MT	Delay matching, HS & LS turn-on/off		---	---	10	

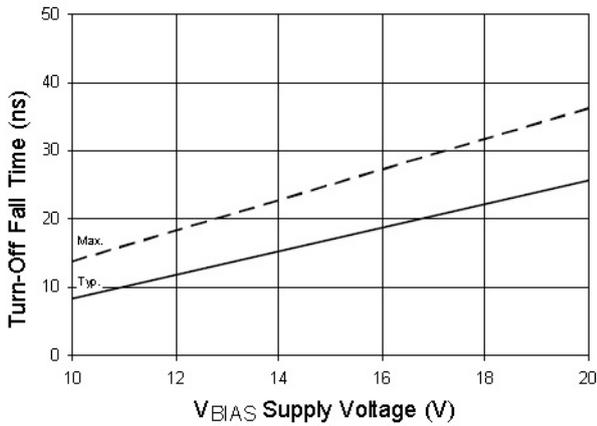
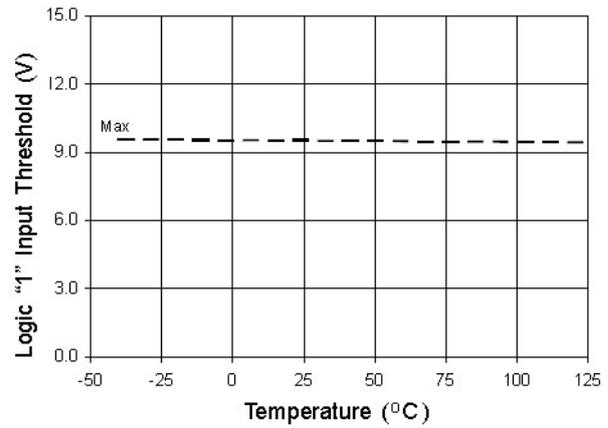
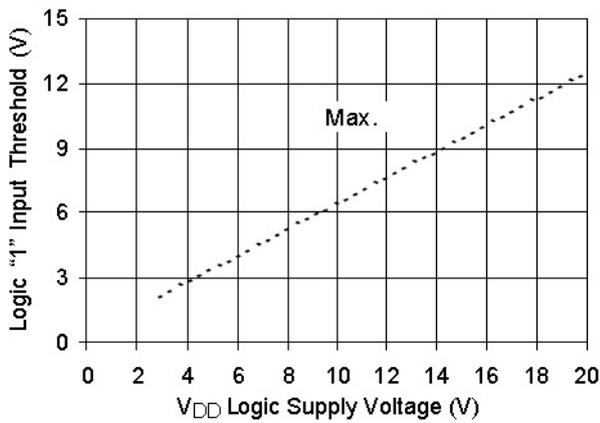
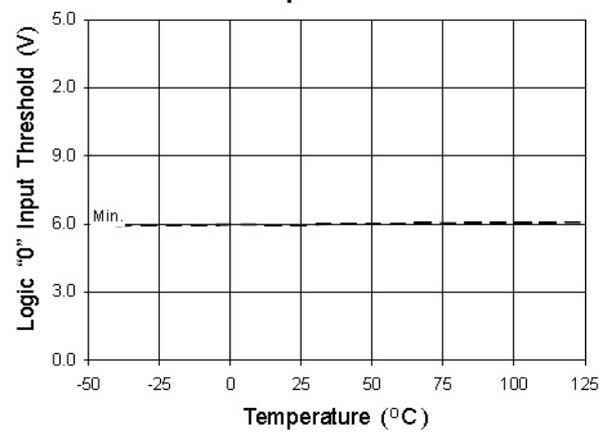
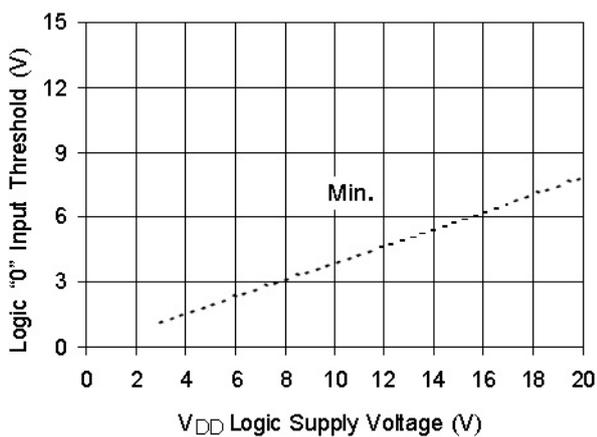
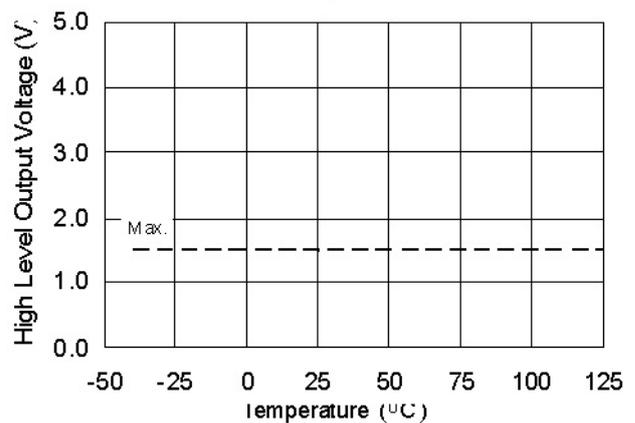
**STATIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all three logic input leads: HIN, LIN, and SD. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

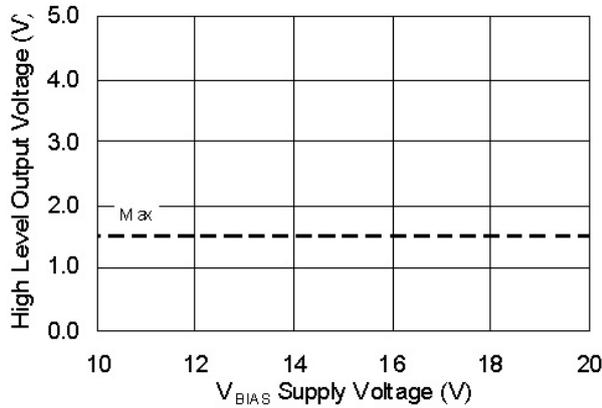
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IH}$	Logic "1" input voltage	$V_{CC} = 10\text{ V to }20\text{ V}$	10.2	---	---	V
$V_{IL}$	Logic "0" input voltage		---	---	5.0	
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2\text{ mA}$	---	---	1.4	
$V_{OL}$	Low level output voltage, $V_O$		---	0.02	0.15	
$I_{LK}$	Offset supply leakage current	$V_B = V_S = 600\text{ V}$	---	---	50	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	$V_{IN} = 0\text{ V or }5\text{ V}$	---	65	120	
$I_{QCC}$	Quiescent $V_{CC}$ supply current		---	300	550	
$I_{QDD}$	Quiescent $V_{DD}$ supply current		---	15	30	
$I_{IN+}$	Logic "1" input bias current	$V_{IN} = 5\text{ V}$	---	25	40	
$I_{IN-}$	Logic "0" input bias current	$V_{IN} = 0\text{ V}$	---	---	5	
$V_{BSUV+}$	$V_{BS}$ supply undervoltage positive going threshold		7.5	8.9	9.7	V
$V_{BSUV-}$	$V_{BS}$ supply undervoltage negative going threshold		7.4	8.2	9.4	
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold		7.5	8.9	9.7	V
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold		7.4	8.2	9.4	
$I_{O+}$	Output high short circuit pulsed current	$V_O = 0\text{ V}$ $V_{IN} = \text{Logic "1"}$ $PW \leq 10\text{ }\mu\text{s}$	2.0	2.5		A
$I_{O-}$	Output low short circuit pulsed current	$V_O = 15\text{ V}$ $V_{IN} = \text{Logic "0"}$ $PW \leq 10\text{ }\mu\text{s}$	2.0	2.5		


**Figure 1. Input/Output Timing Diagram**

**Figure 2. Floating Supply Voltage Transient Test Circuit**

**Figure 3. Switching Time Test Circuit**

**Figure 4. Switching Time Waveform Definition**

**Figure 5. Shutdown Waveform Definitions**

**Figure 6. Delay Matching Waveform Definitions**

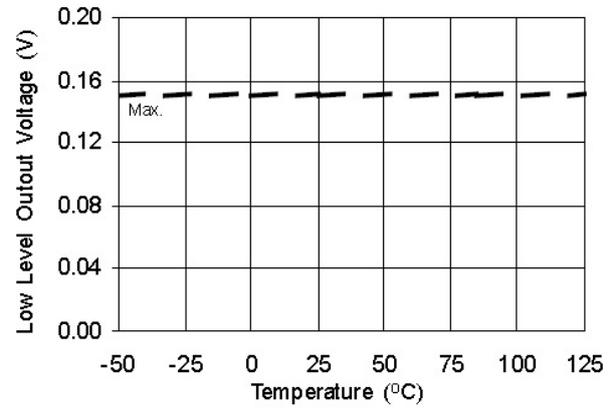

**Figure 7A. Turn-On Time vs. Temperature**

**Figure 7B. Turn-On Time vs. Supply Voltage**

**Figure 7C. Turn-On Time vs. V<sub>DD</sub> Supply Voltage**

**Figure 8A. Turn-Off Time vs. Temperature**

**Figure 8B. Turn-Off Time vs. Supply Voltage**

**Figure 8C. Turn-Off Time vs. V<sub>DD</sub> Supply Voltage**


**Figure 9A. Shutdown Time vs. Temperature**

**Figure 9B. Shutdown Time vs. Supply Voltage**

**Figure 9C. Shutdown Time vs. VDD Supply Voltage**

**Figure 10A. Turn-On Rise Time vs. Temperature**

**Figure 10B. Turn-On Rise Time vs. Voltage**

**Figure 11A. Turn-Off Fall Time vs. Temperature**

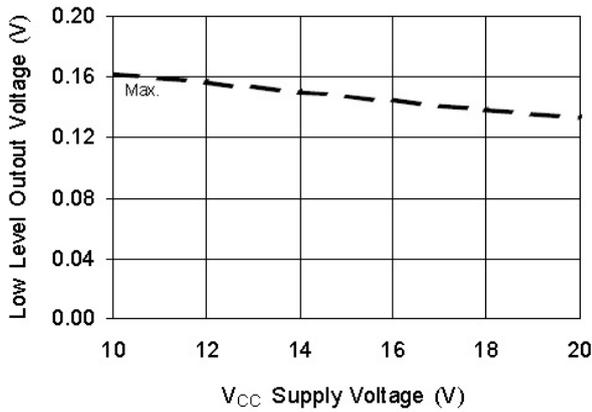

**Figure 11B. Turn-Off Fall Time vs. Voltage**

**Figure 12A. Logic "1" Input Threshold vs. Temperature**

**Figure 12B. Logic "1" Input Threshold vs. Voltage**

**Figure 13A. Logic "0" Input Threshold vs. Temperature**

**Figure 13B. Logic "0" Input Threshold vs. Voltage**

**Figure 14A. High Level Output Voltage vs. Temperature (I<sub>o</sub> = 0 mA)**



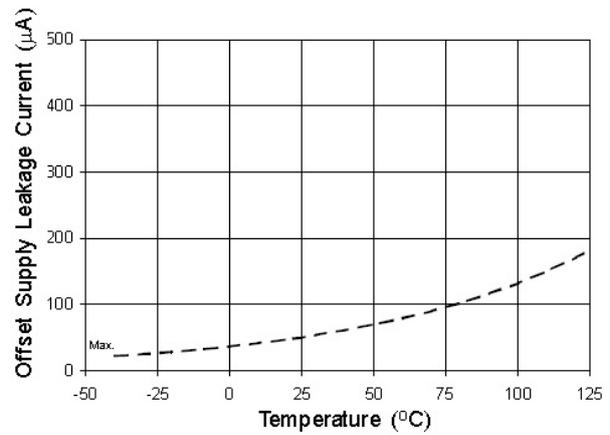
**Figure 14B. High Level Output Voltage vs. Supply Voltage ( $I_o = 0$  mA)**



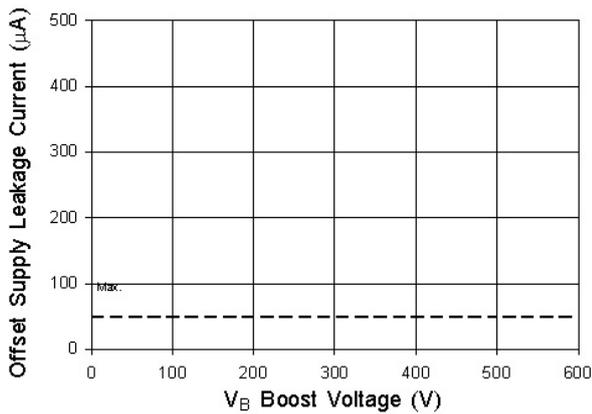
**Figure 15A. Low Level Output vs. Temperature**



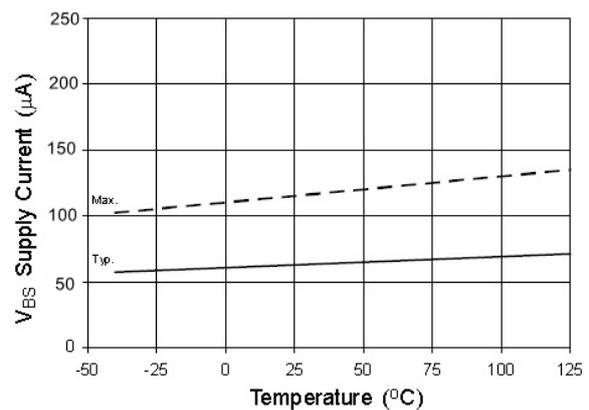
**Figure 15B. Low Level Output vs. Supply Voltage**



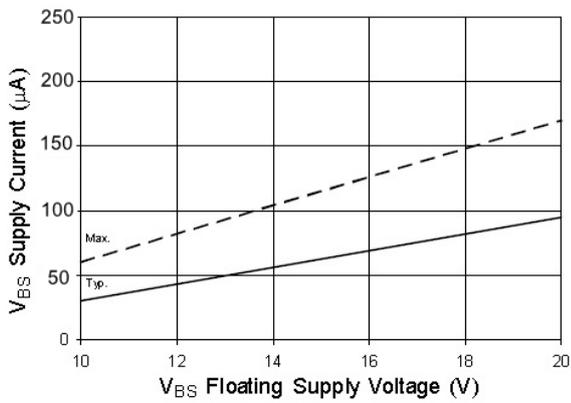
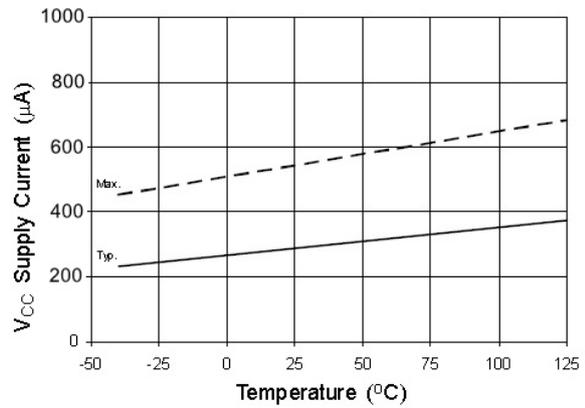
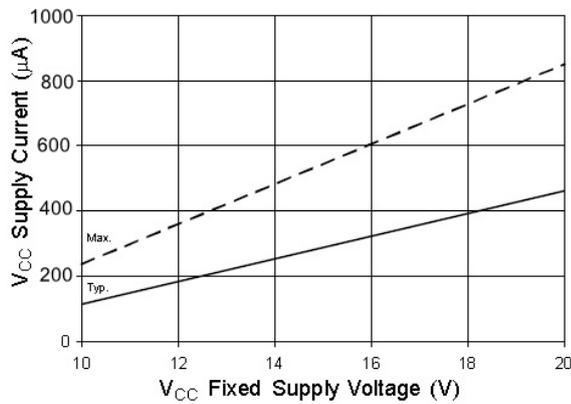
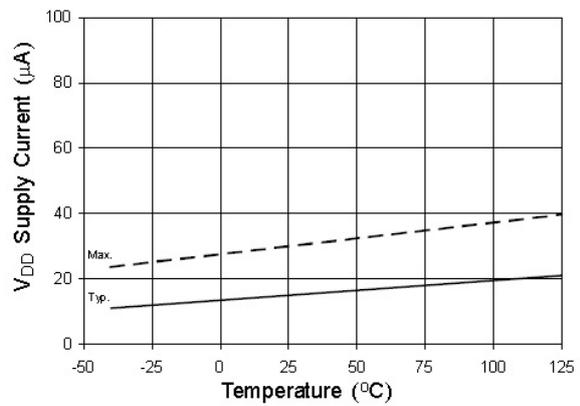
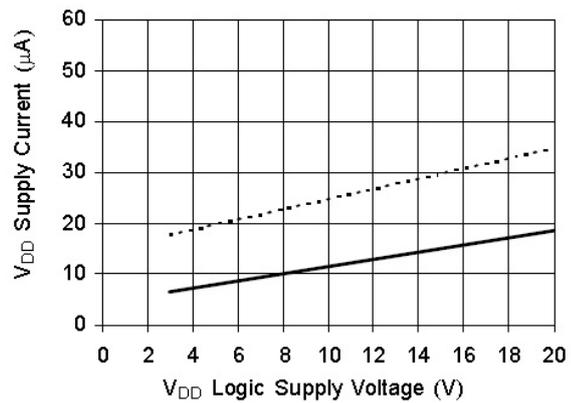
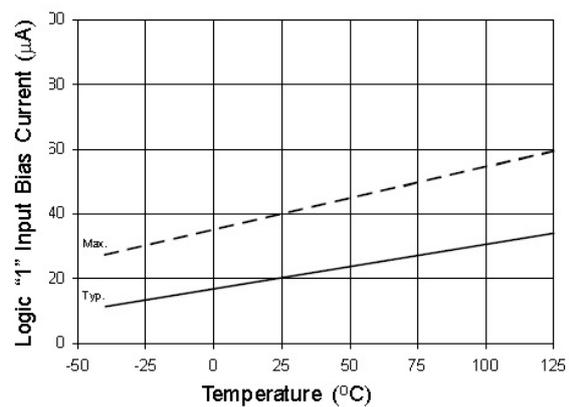
**Figure 16A. Offset Supply Current vs. Temperature**

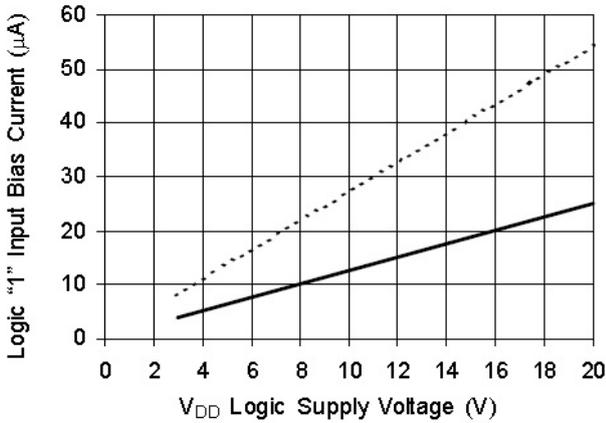


**Figure 16B. Offset Supply Current vs. Voltage**

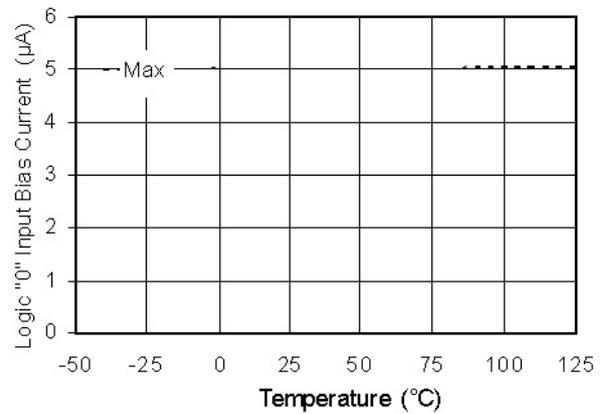


**Figure 17A. V<sub>BS</sub> Supply Current vs. Temperature**

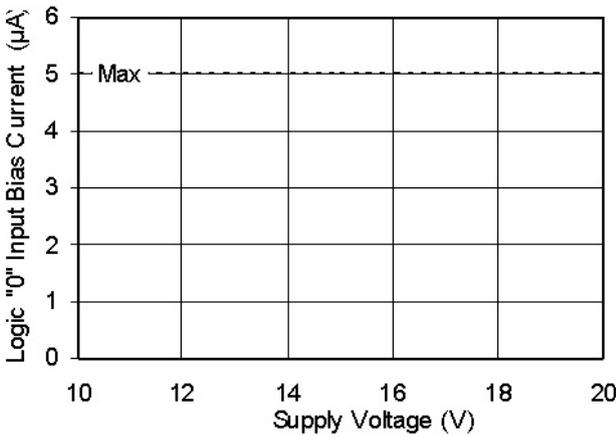

**Figure 17B. V<sub>BS</sub> Supply Current vs. Voltage**

**Figure 18A. V<sub>CC</sub> Supply Current vs. Temperature**

**Figure 18B. V<sub>CC</sub> Supply Current vs. Voltage**

**Figure 19A. V<sub>DD</sub> Supply Current vs. Temperature**

**Figure 19B. V<sub>DD</sub> Supply Current vs. V<sub>DD</sub> Voltage**

**Figure 20A. Logic "1" Input Current vs. Temperature**



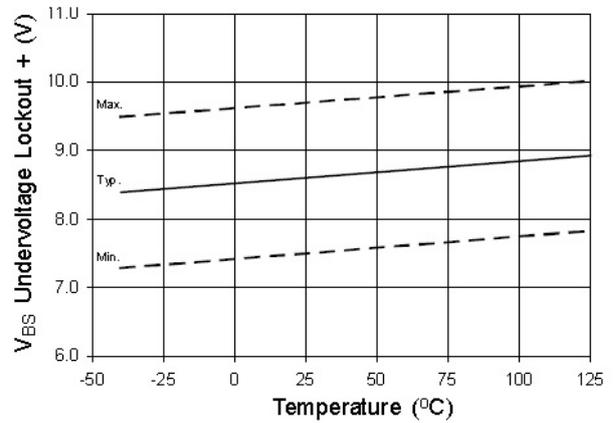
**Figure 20B. Logic "1" Input Current vs. V<sub>DD</sub> Voltage**



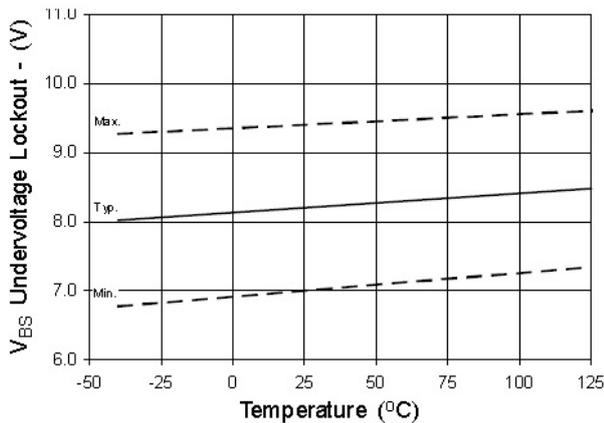
**Figure 21A. Logic "0" Input Bias Current vs. Temperature**



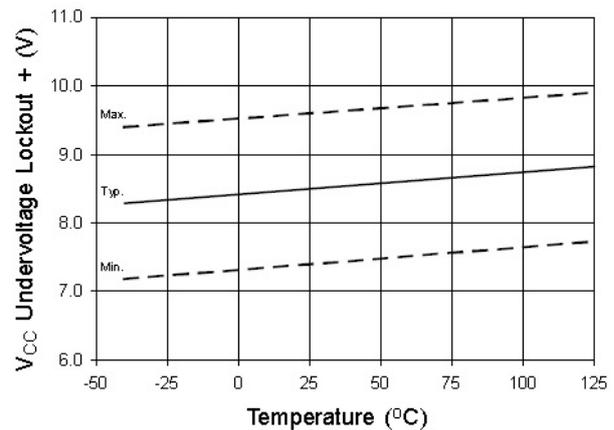
**Figure 21B. Logic "0" Input Bias Current vs. Voltage**



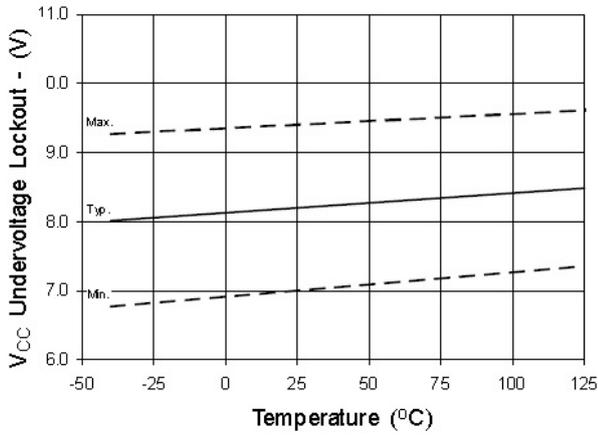
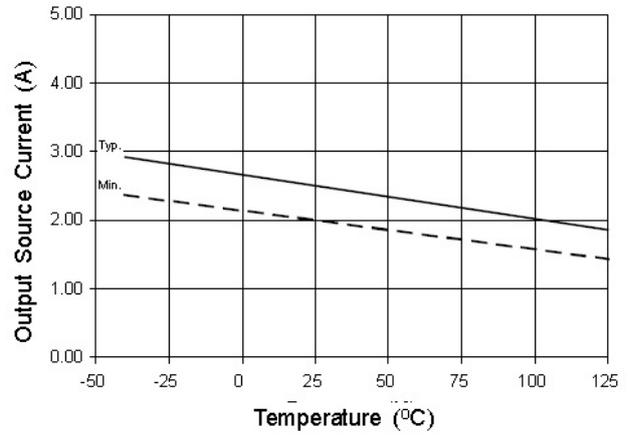
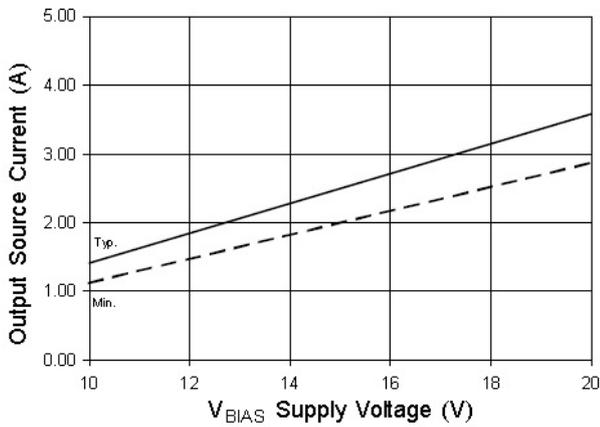
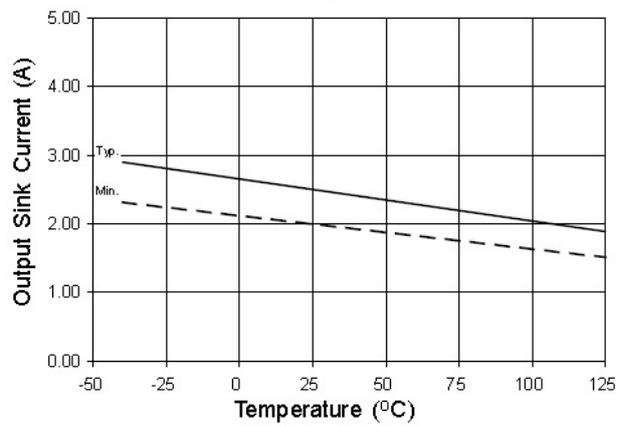
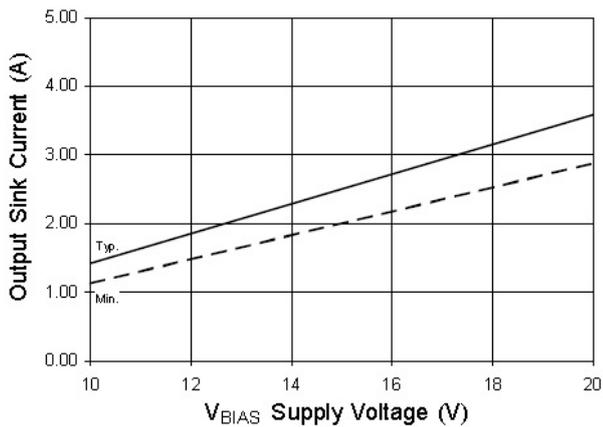
**Figure 22. V<sub>BS</sub> Undervoltage (+) vs. Temperature**

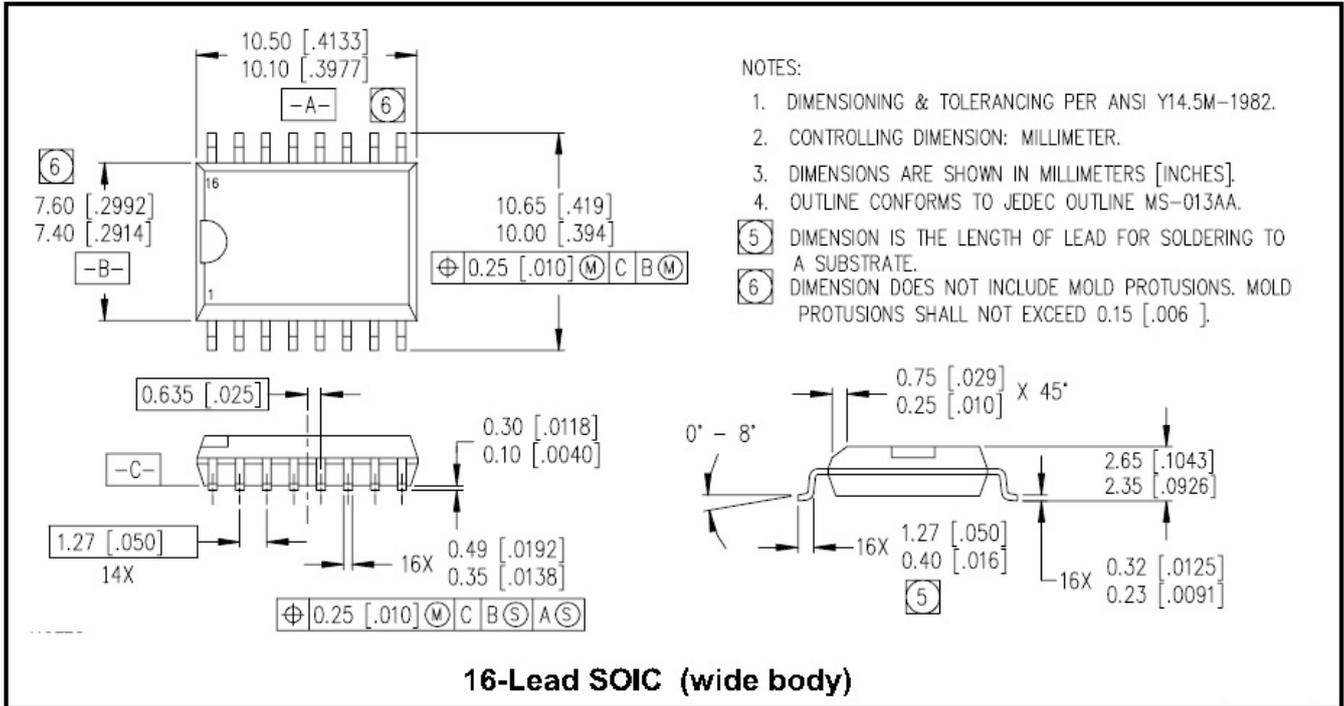


**Figure 23. V<sub>BS</sub> Undervoltage (-) vs. Temperature**



**Figure 24. V<sub>CC</sub> Undervoltage (+) vs. Temperature**


**Figure 25. V<sub>CC</sub> Undervoltage (-) vs. Temperature**

**Figure 26A. Output Source Current vs. Temperature**

**Figure 26B. Output Source Current vs. Voltage**

**Figure 27A. Output Sink Current vs. Temperature**

**Figure 27B. Output Sink Current vs. Voltage**

**PACKAGE CASE OUTLINES**


**Revision History**

Note: page numbers for previous revisions may differ from page numbers in current version

<b>Page or Item</b>	<b>Subjects (major changes since previous revision)</b>
<b>Rev 1.0 datasheet, 2019-8-27</b>	
Whole document	New company logo released
Page 1	Remove "May 2019"