27256
256K (32K x 8) PRODUCTION AND UV ERASABLE PROMS

- **New Quick-Pulse Programming™ Algorithm for Plastic P27256**
  - **4 Second Programming**
  - **int$_e$ligent Programming™ Algorithm Compatible**
- **Fast Access Time**
  - **170 ns D27256-1**
  - **200 ns P27256-2**
- **int$_e$ligent Identifier™ Mode**
- **Plastic Production P27256 is Compatible with Auto-Insertion Equipment**
- **Moisture Resistant**
- **Industry Standard Pinout . . . JEDEC Approved . . . 28 Lead Cerdip and Plastic Package**

  (See Packaging Spec, Order #231369)

The Intel 27256 is a 5V only, 262,144-bit Ultraviolet Erasable (Cerdip)/plastic production (P27256) electrically programmable read-only memory (EPROM). Organized as 32K words by 8 bits, individual bytes can be accessed in less than 170 ns (27256-1). This is compatible with high performance microprocessors, such as the Intel iAPX 186, allowing full speed operation without the addition of performance-degrading WAIT states. The 27256 is also directly compatible with Intel's 8051 family of microcontrollers.

The Plastic P27256 is ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P27256 to be programmed within four seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment.

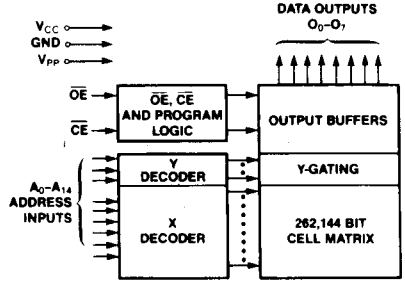
The 27256 enables implementation of new, advanced systems with firmware-intensive architectures. The combination of the 27256's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems.

The 27256's large storage capability of 32 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27256 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and elminates the need for time-consuming disk accesses and downloads.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27256 is manufactured using Intel's advanced HMOS*II-E technology.

*HMOS is a patented process of Intel Corporation.



290097-1

Figure 1. Block Diagram

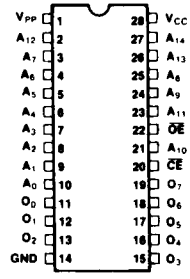
September 1989
Order Number: 290097-004

Pin Names

A_0–A_{14}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
N.C.	No Connect

27512 27C512	27128A 27C128	2764A 27C64 87C64	2732A	2716
A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27256
P27256



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2716	2732A	2764A 27C64 87C64	27182A 27C128	27512 27C512
		V_{CC} / $\overline{PGM}$	V_{CC} / $\overline{PGM}$	V_{CC}
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE:
Intel"Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the P27256 pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

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EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27256 VERSIONS

Packaging Options	
Speed Versions	Cerdip
-20	Q, T, L

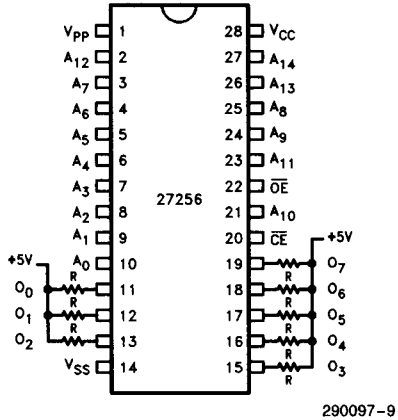
READ OPERATION

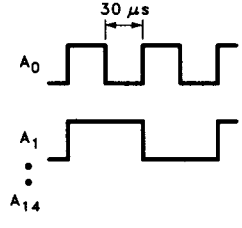
D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27256 LD27256		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC}(1)	V_{CC} Active Current (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.





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Binary Sequence from A_0 to A_{14}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C

Storage Temperature ..... −65°C to +125°C

All Input or Output Voltages with
Respect to Ground ..... −0.6V to +6.25V

Voltage on Pin 24 with
Respect to Ground ..... −0.6V to +13.5V

V_{PP} Supply Voltage with Respect
to Ground ..... −0.6V to +14.0V

V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7.0V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	27256-1, 27256-2, 27256-20, P27256-2 Limits			27256-25, 27256, P27256-25, P27256 Limits			Unit	Test Conditions
		Min	Typ (3)	Max	Min	Typ (3)	Max		
I_{LI}	Input Load Current			10			10	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10			10	µA	V_{OUT} = 0V to V_{CC}
I_{PP_1}(2)	V_{PP} Current Read/Standby			5			5	mA	V_{PP} = 5.5V
I_{SB}(2)	V_{CC} Current Standby		25	50		20	40	mA	$\overline{CE}$ = V_{IH}
I_{CC1}(2)	V_{CC} Current Active		55	125		45	100	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} V_{PP} = V_{CC}
V_{IL}	Input Low Voltage	−0.1		+0.8	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −400 µA
V_{PP}(2)	V_{PP} Read Voltage	3.8		V_{CC}	3.8		V_{CC}	V	V_{CC} = 5.0V ± 0.25V

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READ OPERATION

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Versions[5]	$V_{CC} \pm 5\%$	27256-1		27256-2 P27256-2		27256 P27256		Unit	Test Conditions
	$V_{CC} \pm 10\%$			27256-20		27256-25 P27256-25			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
t_{ACC}	Address to Output Delay		170		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		170		200		250	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		70		75		100	ns	$\overline{CE} = V_{IL}$
t_{DF}[4]	$\overline{OE}$ High to Output Float	0	35	0	55	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}[4]	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	

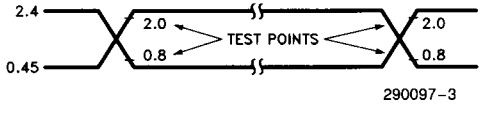
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram.
5. Packaging Options: No prefix = Cerdip; P = Plastic DIP.

CAPACITANCE[2] ($T_A = 25°C$, f = 1 MHz)

Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

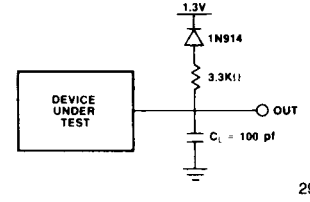
NOTES:
1. $T_A = 25°C$, $V_{CC} = 5.0V$.
2. This parameter is only sampled and is not 100% tested.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. Testing; Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance