

# PS21965-T/-AT/-CT/-TW

TRANSFER-MOLD TYPE  
INSULATED TYPE

## PS21965-T



### INTEGRATED POWER FUNCTIONS

600V/20A low-loss CSTBT™ inverter bridge for three phase DC-to-AC power conversion

### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

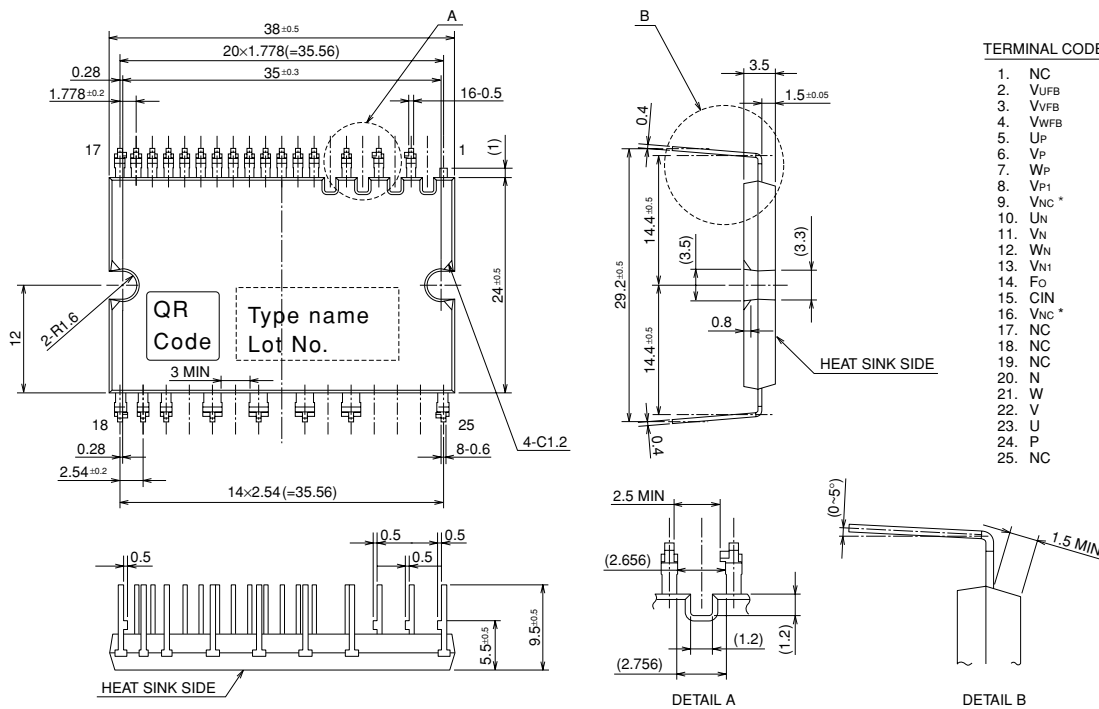
- For upper-leg IGBTs : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC), Over temperature protection (OT).
- Fault signaling : Corresponding to an SC fault (Lower-leg IGBT), a UV fault (Lower-side supply) or an OT fault (LVIC temperature).
- Input interface : 3V, 5V line (High Active).
- UL Approved : Yellow Card No. E80276

## APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES (PS21965-T)

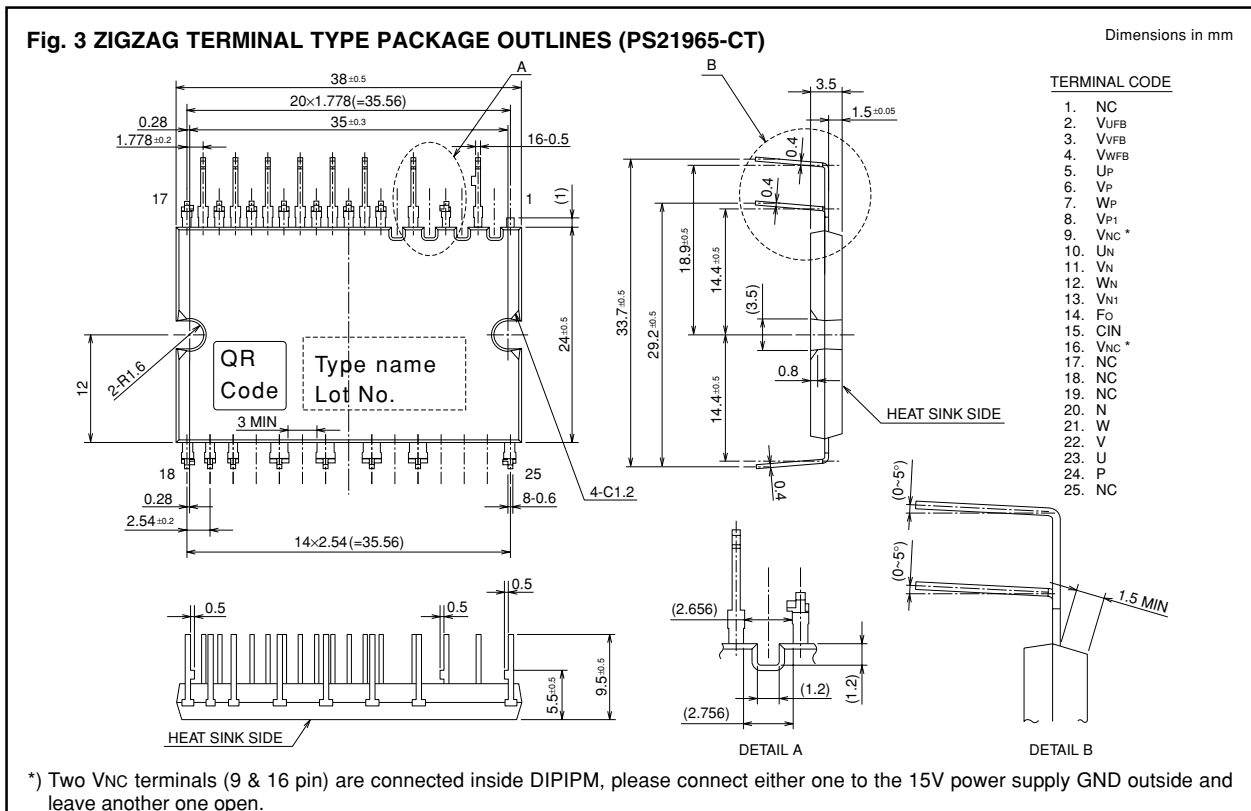
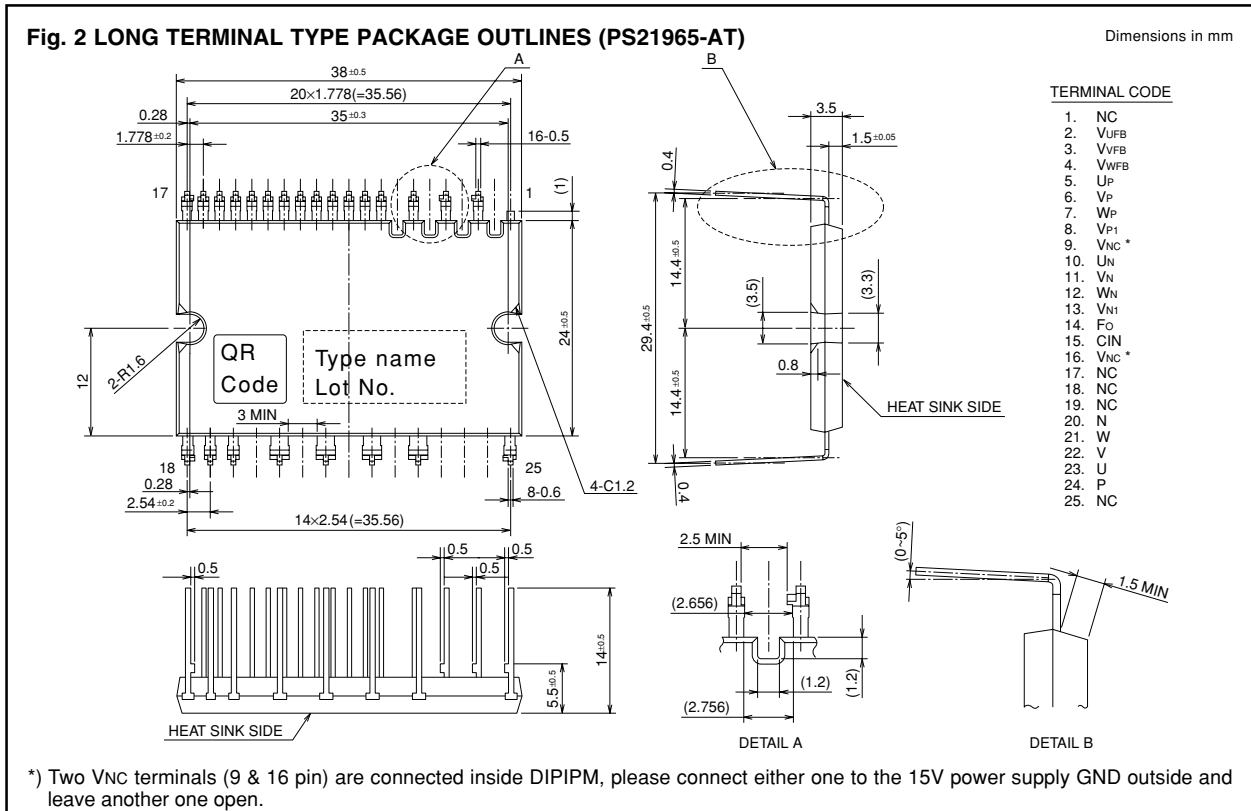
Dimensions in mm



\*) Two V<sub>NC</sub> terminals (9 & 16 pin) are connected inside DIPIMP, please connect either one to the 15V power supply GND outside and leave another one open.

# PS21965-T/-AT/-CT/-TW

TRANSFER-MOLD TYPE  
INSULATED TYPE

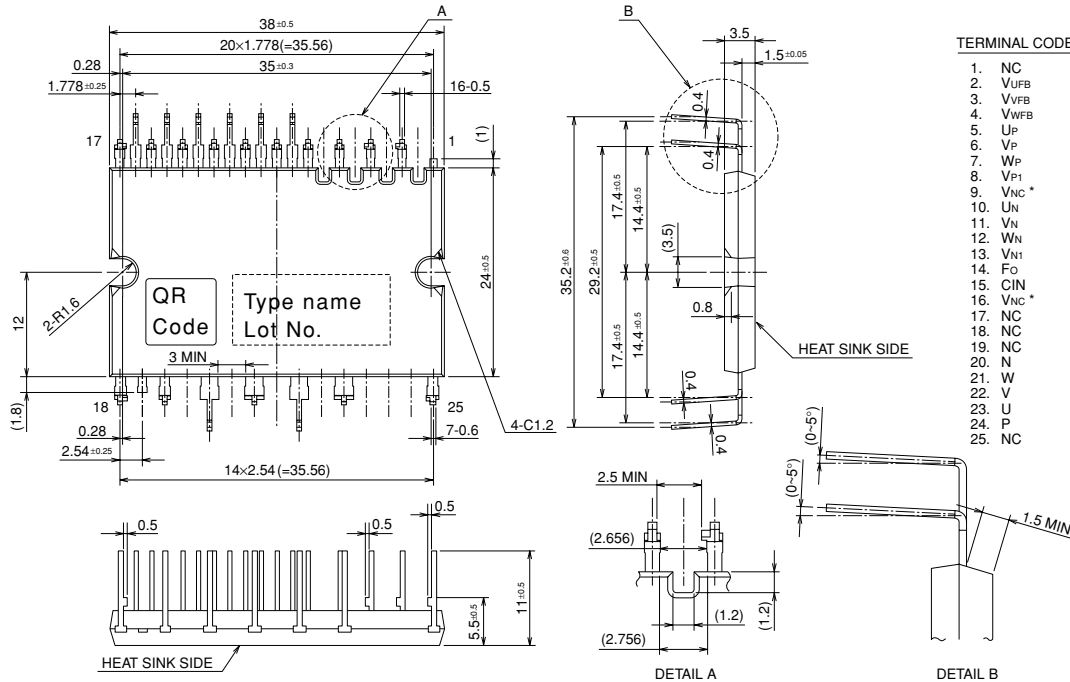


PS21965-T/-AT/-CT/-TW

TRANSFER-MOLD TYPE  
INSULATED TYPE

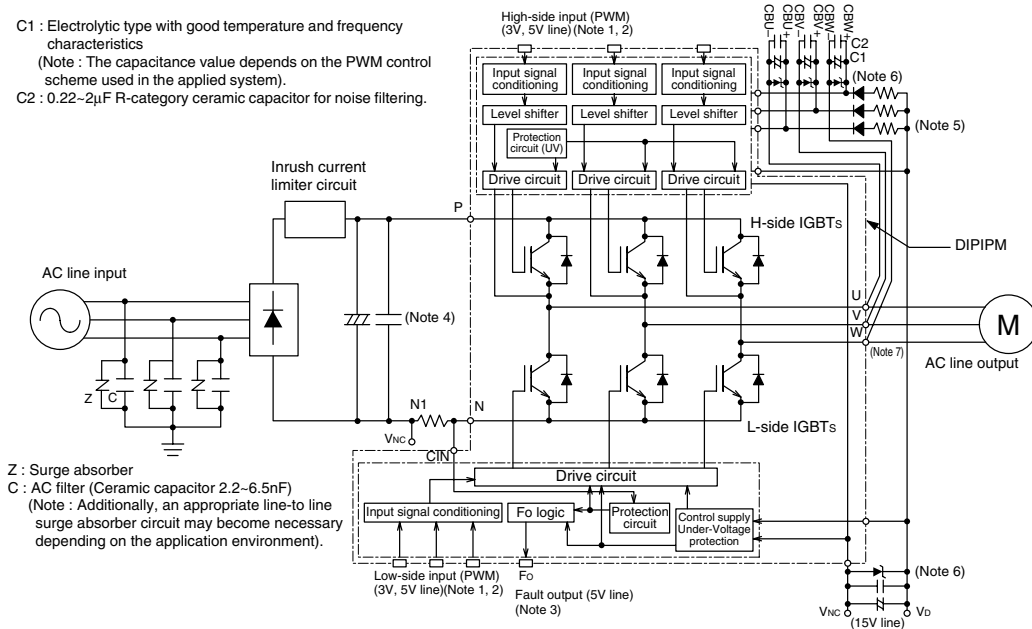
Fig. 4 BOTH SIDES ZIGZAG TERMINAL TYPE PACKAGE OUTLINES (PS21965-TW)

Dimensions in mm



\*) Two V<sub>NC</sub> terminals (9 & 16 pin) are connected inside DIPIM, please connect either one to the 15V power supply GND outside and leave another one open.  
QR Code is registered trademark of DENSO WAVE INCORPORATED in Japan and other countries.

Fig. 5 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

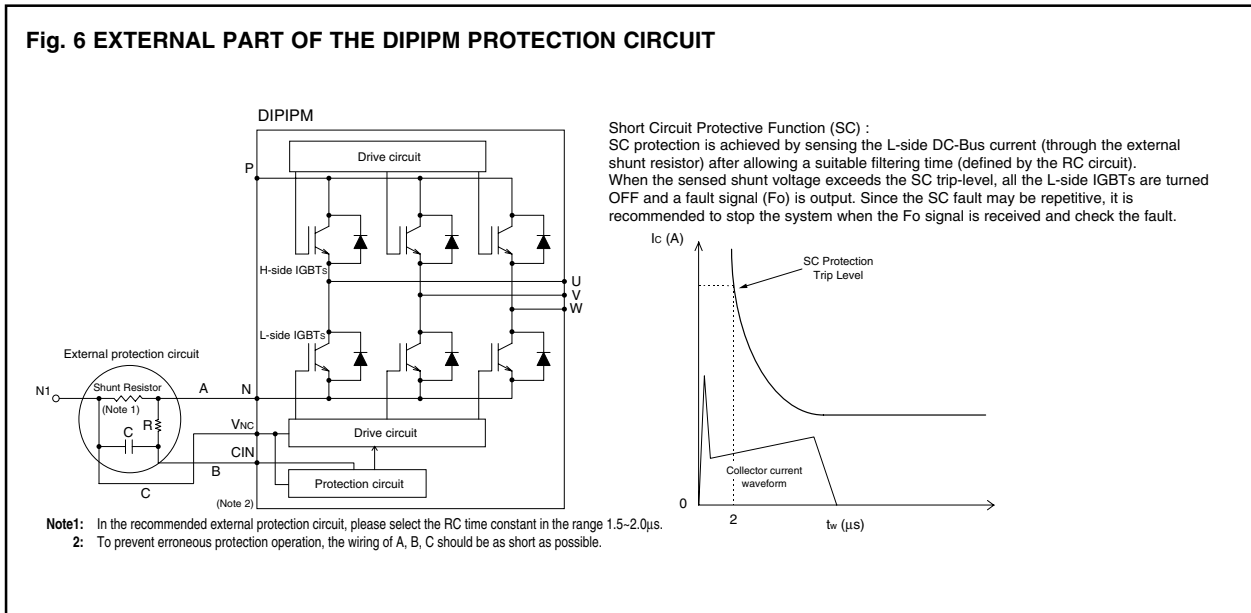


- Note1:** Input logic is high-active. There is a 3.3kΩ (min) pull-down resistor built-in each input circuit. When using an external CR filter, please make it satisfy the input threshold voltage.
- 2:** By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible. (see also Fig. 11)
- 3:** This output is open drain type. The signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor. (see also Fig. 11)
- 4:** The wiring between the power DC link capacitor and the P, N1 terminals should be as short as possible to protect the DIPIM against catastrophic high surge voltages. For extra precaution, a small film type snubber capacitor (0.1-0.22μF, high voltage type) is recommended to be mounted close to these P & N1 DC power input pins.
- 5:** High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.
- 6:** It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- 7:** Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.

**PS21965-T/-AT/-CT/-TW**

**TRANSFER-MOLD TYPE  
INSULATED TYPE**

**Fig. 6 EXTERNAL PART OF THE DIIPIM PROTECTION CIRCUIT**



**MAXIMUM RATINGS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)

**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P-N	450	V
VCC(surge)	Supply voltage (surge)	Applied between P-N	500	V
VCEs	Collector-emitter voltage		600	V
$\pm I_c$	Each IGBT collector current	$T_c = 25^\circ\text{C}$	20	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_c = 25^\circ\text{C}$ , less than 1ms	40	A
Pc	Collector dissipation	$T_c = 25^\circ\text{C}$ , per 1 chip	35.7	W
Tj	Junction temperature	(Note 1)	-20~+125	$^\circ\text{C}$

**Note 1 :** The maximum junction temperature rating of the power chips integrated within the DIIPIM is  $150^\circ\text{C}$  (@  $T_c \leq 100^\circ\text{C}$ ). However, to ensure safe operation of the DIIPIM, the average junction temperature should be limited to  $T_{j(ave)} \leq 125^\circ\text{C}$  (@  $T_c \leq 100^\circ\text{C}$ ).

**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition	Ratings	Unit
V <sub>D</sub>	Control supply voltage	Applied between VP1-VNC, VN1-VNC	20	V
V <sub>DB</sub>	Control supply voltage	Applied between VUFB-U, VVFB-V, VWFB-W	20	V
V <sub>IN</sub>	Input voltage	Applied between UP, VP, WP, UN, VN, WN-VNC	-0.5~V <sub>D</sub> +0.5	V
V <sub>FO</sub>	Fault output supply voltage	Applied between FO-VNC	-0.5~V <sub>D</sub> +0.5	V
I <sub>FO</sub>	Fault output current	Sink current at Fo terminal	1	mA
V <sub>SC</sub>	Current sensing input voltage	Applied between CIN-VNC	-0.5~V <sub>D</sub> +0.5	V

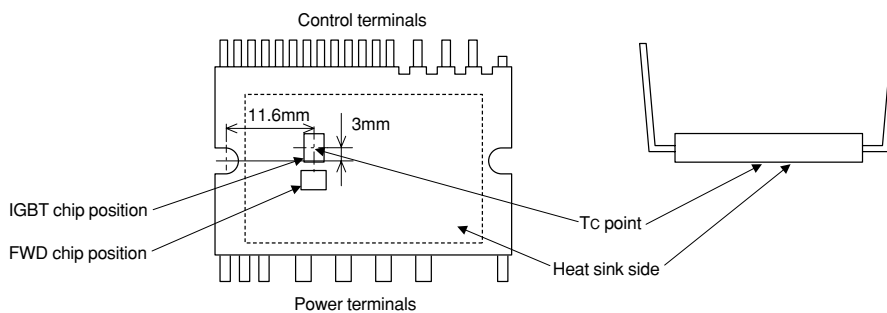
# PS21965-T/-AT/-CT/-TW

TRANSFER-MOLD TYPE  
INSULATED TYPE

## TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V <sub>CC(PROT)</sub>	Self protection supply voltage limit (short circuit protection capability)	V <sub>D</sub> = 13.5~16.5V, Inverter part T <sub>j</sub> = 125°C, non-repetitive, less than 2μs	400	V
T <sub>C</sub>	Module case operation temperature	(Note 2)	-20~+100	°C
T <sub>stg</sub>	Storage temperature		-40~+125	°C
V <sub>iso</sub>	Isolation voltage	60Hz, Sinusoidal, 1 minute, Between pins and heat-sink plate	1500	V <sub>rms</sub>

**Note 2:** T<sub>C</sub> measurement point



## THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R <sub>th(j-c)Q</sub>	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	2.8	°C/W
R <sub>th(j-c)F</sub>		Inverter FWD part (per 1/6 module)	—	—	3.9	°C/W

**Note 3:** Grease with good thermal conductivity should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat-sink.

The contacting thermal resistance between DIPIPM case and heat sink (R<sub>th(c-f)</sub>) is determined by the thickness and the thermal conductivity of the applied grease. For reference, R<sub>th(c-f)</sub> (per 1/6 module) is about 0.3°C/W when the grease thickness is 20μm and the thermal conductivity is 1.0W/m·k.

## ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C, unless otherwise noted)

### INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V <sub>CE(sat)</sub>	Collector-emitter saturation voltage	V <sub>D</sub> = V <sub>DB</sub> = 15V V <sub>IN</sub> = 5V	—	1.70	2.20	V
		I <sub>C</sub> = 20A, T <sub>j</sub> = 25°C I <sub>C</sub> = 20A, T <sub>j</sub> = 125°C	—	1.80	2.30	
V <sub>EC</sub>	FWD forward voltage	T <sub>j</sub> = 25°C, -I <sub>C</sub> = 20A, V <sub>IN</sub> = 0V	—	1.90	2.40	V
t <sub>on</sub>	Switching times	V <sub>CC</sub> = 300V, V <sub>D</sub> = V <sub>DB</sub> = 15V I <sub>C</sub> = 20A, T <sub>j</sub> = 125°C, V <sub>IN</sub> = 0 ↔ 5V Inductive load (upper-lower arm)	0.70	1.30	1.90	μs
t <sub>tr</sub>			—	0.30	—	μs
t <sub>c(on)</sub>			—	0.50	0.75	μs
t <sub>off</sub>			—	1.60	2.20	μs
t <sub>c(off)</sub>			—	0.40	0.75	μs
I <sub>CES</sub>	Collector-emitter cut-off current	V <sub>CE</sub> = V <sub>CES</sub>	—	—	1	mA
		T <sub>j</sub> = 25°C T <sub>j</sub> = 125°C	—	—	10	

# PS21965-T/-AT/-CT/-TW

TRANSFER-MOLD TYPE  
INSULATED TYPE

## CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I <sub>D</sub>	Circuit current	V <sub>D</sub> = V <sub>DB</sub> = 15V V <sub>IN</sub> = 5V	Total of V <sub>P1</sub> -V <sub>NC</sub> , V <sub>N1</sub> -V <sub>NC</sub>	—	—	2.80	mA
			V <sub>UFB</sub> -U, V <sub>VFB</sub> -V, V <sub>WFB</sub> -W	—	—	0.55	mA
		V <sub>D</sub> = V <sub>DB</sub> = 15V V <sub>IN</sub> = 0V	Total of V <sub>P1</sub> -V <sub>NC</sub> , V <sub>N1</sub> -V <sub>NC</sub>	—	—	2.80	mA
			V <sub>UFB</sub> -U, V <sub>VFB</sub> -V, V <sub>WFB</sub> -W	—	—	0.55	mA
V <sub>FOH</sub>	Fault output voltage	V <sub>SC</sub> = 0V, F <sub>O</sub> terminal pull-up to 5V by 10kΩ	4.9	—	—	V	
V <sub>FOL</sub>		V <sub>SC</sub> = 1V, I <sub>FO</sub> = 1mA	—	—	0.95	V	
V <sub>SC(ref)</sub>	Short circuit trip level	T <sub>j</sub> = 25°C, V <sub>D</sub> = 15V (Note 4)	0.43	0.48	0.53	V	
I <sub>IN</sub>	Input current	V <sub>IN</sub> = 5V	0.70	1.00	1.50	mA	
OT <sub>t</sub>	Over temperature protection (Note 5)	V <sub>D</sub> = 15V, At temperature of LVIC	Trip level	100	120	140	°C
OT <sub>rh</sub>			Trip/reset hysteresis	—	10	—	
UVDB <sub>t</sub>	Control supply under-voltage protection	T <sub>j</sub> ≤ 125°C	Trip level	10.0	—	12.0	V
UVDB <sub>r</sub>			Reset level	10.5	—	12.5	V
UV <sub>Dt</sub>			Trip level	10.3	—	12.5	V
UV <sub>Dr</sub>			Reset level	10.8	—	13.0	V
t <sub>FO</sub>	Fault output pulse width	(Note 6)	20	—	—	μs	
V <sub>th(on)</sub>	ON threshold voltage	Applied between U <sub>P</sub> , V <sub>P</sub> , W <sub>P</sub> , U <sub>N</sub> , V <sub>N</sub> , W <sub>N</sub> -V <sub>NC</sub>	—	2.1	2.6	V	
V <sub>th(off)</sub>	OFF threshold voltage		0.8	1.3	—	V	
V <sub>th(hys)</sub>	ON/OFF threshold hysteresis voltage		0.35	0.65	—	V	

**Note 4 :** Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

**5 :** Over temperature protection (OT) outputs fault signal, when the LVIC temperature exceeds OT trip temperature level (OT<sub>t</sub>). In that case if the heat sink comes off DIPIPM or fixed loosely, don't reuse that DIPIPM. (There is a possibility that junction temperature of power chips exceeded maximum T<sub>j</sub> (150°C)).

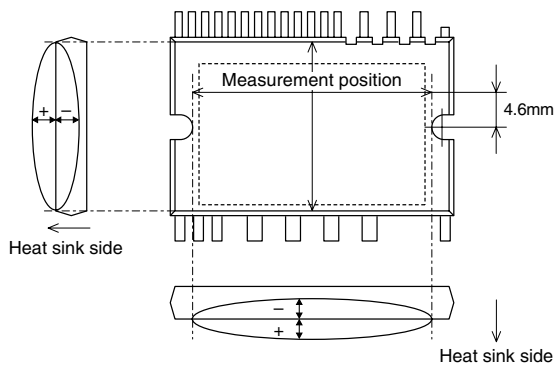
**6 :** Fault signal is asserted only corresponding to a SC, a UV or an OT failure at lower side, and the FO pulse width is different for each failure modes. For SC failure, FO output is with a fixed width of 20μsec(min), but for UV or OT failure, FO output continuously during the whole UV or OT period, however, the minimum FO pulse width is 20μsec(min) for very short UV or OT period less than 20μsec.

## MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Unit
		Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 7) Recommended : 0.69 N·m	0.59	—	0.78	N·m
Weight		—	10	—	g
Heat-sink flatness	(Note 8)	-50	—	100	μm

**Note 7 :** Plain washers (ISO 7089~7094) are recommended.

**Note 8 :** Flatness measurement position



# PS21965-T/-AT/-CT/-TW

TRANSFER-MOLD TYPE  
INSULATED TYPE

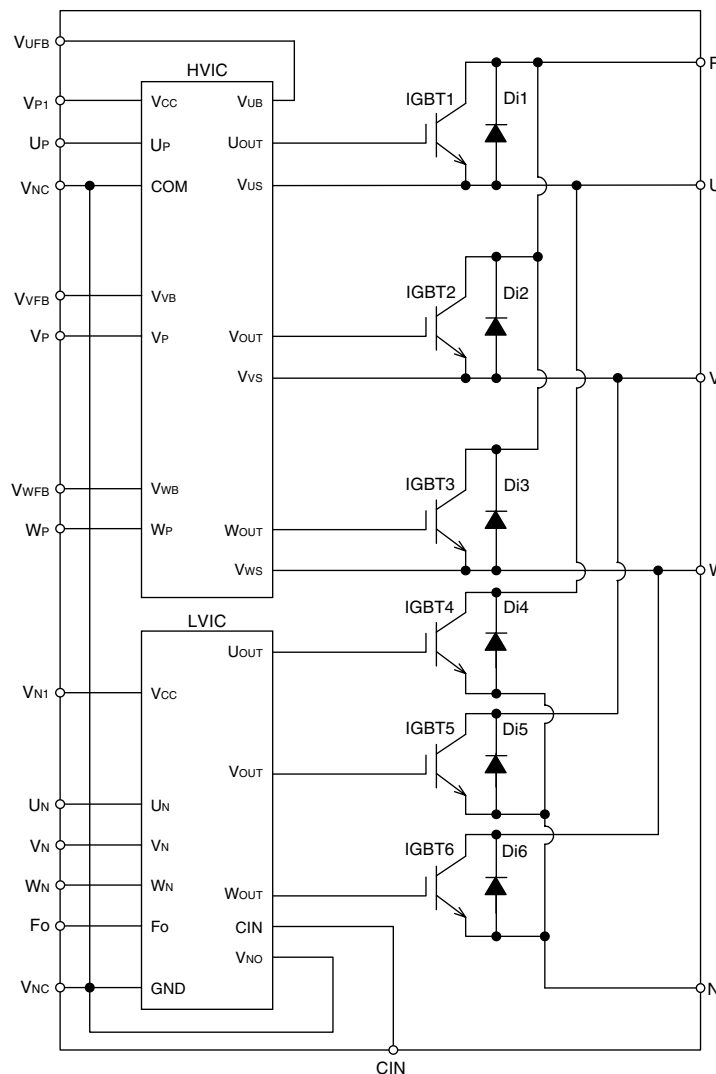
## RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
VCC	Supply voltage	Applied between P-N	0	300	400	V	
VD	Control supply voltage	Applied between VP1-VNC, VN1-VNC	13.5	15.0	16.5	V	
VDB	Control supply voltage	Applied between VUFB-U, VVFB-V, VWFB-W	13.0	15.0	18.5	V	
$\Delta V_D, \Delta V_{DB}$	Control supply variation		-1	—	1	V/ $\mu$ s	
t <sub>dead</sub>	Arm shoot-through blocking time	For each input signal, T <sub>c</sub> ≤ 100°C	1.5	—	—	$\mu$ s	
f <sub>PWM</sub>	PWM input frequency	T <sub>c</sub> ≤ 100°C, T <sub>j</sub> ≤ 125°C	—	—	20	kHz	
I <sub>o</sub>	Allowable r.m.s. current	VCC = 300V, VD = VDB = 15V, P.F = 0.8, sinusoidal PWM, T <sub>j</sub> ≤ 125°C, T <sub>c</sub> ≤ 100°C (Note 9)	f <sub>PWM</sub> = 5kHz	—	—	10.0	Arms
			f <sub>PWM</sub> = 15kHz	—	—	6.0	
PWIN(on)	Allowable minimum input pulse width	(Note 10)	0.5	—	—	$\mu$ s	
PWIN(off)			0.5	—	—		
VNC	VNC variation	Between VNC-N (including surge)	-5.0	—	5.0	V	

**Note 9:** The allowable r.m.s. current value depends on the actual application conditions.

**10:** IPM might not make response if the input signal pulse width is less than the recommended minimum value.

**Fig. 7 THE DIIPM INTERNAL CIRCUIT**



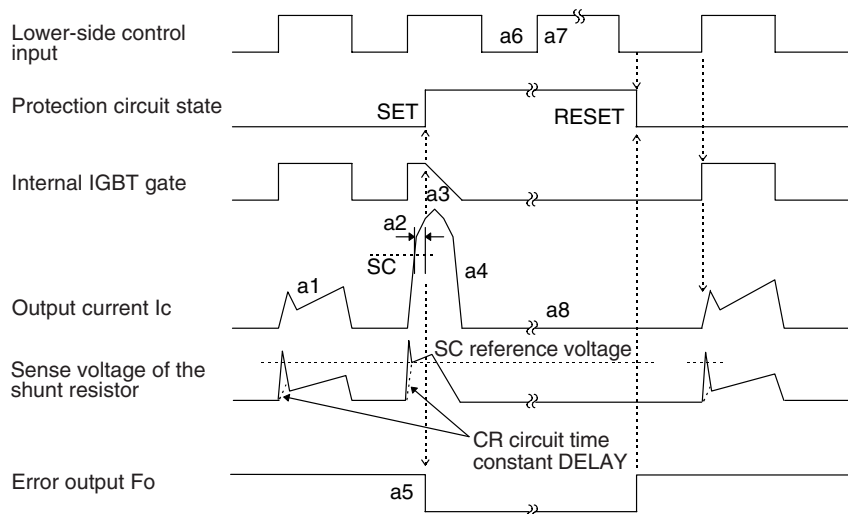
# PS21965-T/-AT/-CT/-TW

TRANSFER-MOLD TYPE  
INSULATED TYPE

**Fig. 8 TIMING CHART OF THE DIIPM PROTECTIVE FUNCTIONS**

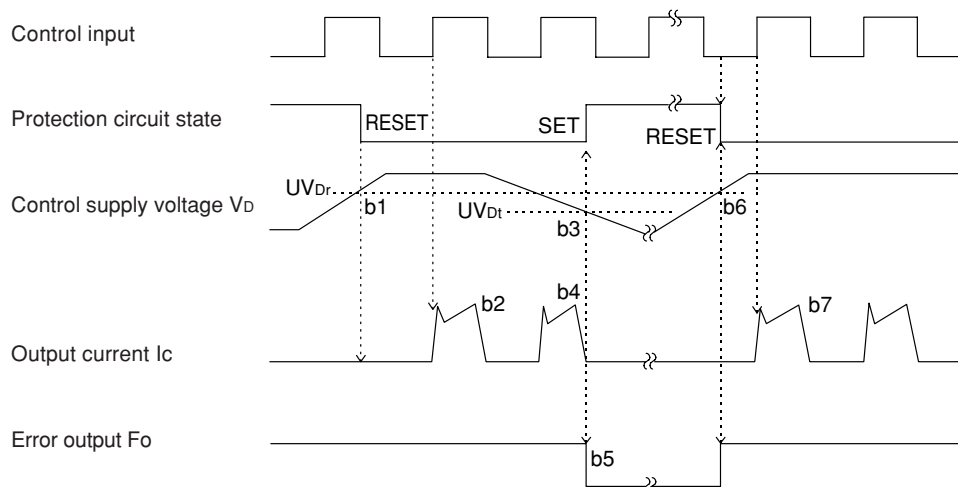
**[A] Short-Circuit Protection (Lower-side only with the external shunt resistor and CR filter)**

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. Fo outputs ( $t_{FO(min)} = 20\mu s$ ).
- a6. Input "L" : IGBT OFF.
- a7. Input "H" : IGBT ON.
- a8. IGBT OFF in spite of input "H".



**[B] Under-Voltage Protection (Lower-side, UV<sub>D</sub>)**

- b1. Control supply voltage rising : After the voltage level reaches UV<sub>Dr</sub>, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV<sub>Dt</sub>).
- b4. IGBT OFF in spite of control input condition.
- b5. Fo outputs ( $t_{FO} \geq 20\mu s$  and Fo outputs continuously during UV period).
- b6. Under voltage reset (UV<sub>Dr</sub>).
- b7. Normal operation : IGBT ON and carrying current.



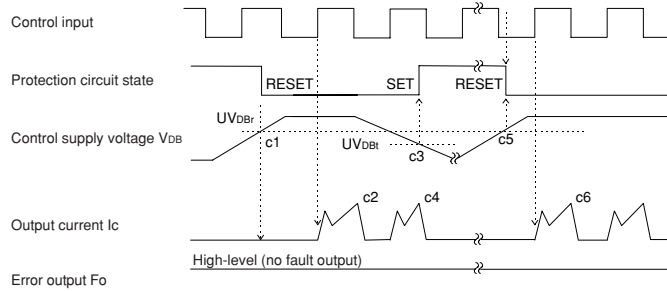


# PS21965-T/-AT/-CT/-TW

TRANSFER-MOLD TYPE  
INSULATED TYPE

## [C] Under-Voltage Protection (Upper-side, UVDB)

- c1. Control supply voltage rising : After the voltage level reaches UVDBr, the circuits start to operate when next input is applied.
- c2. Normal operation : IGBT ON and carrying current.
- c3. Under voltage trip (UVDBt).
- c4. IGBT OFF in spite of control input signal level, but there is no Fo signal outputs.
- c5. Under voltage reset (UVDBr).
- c6. Normal operation : IGBT ON and carrying current.



## [D] Over Temperature Protection (Lower-side, OT)

- d1. Normal operation : IGBT ON and carrying current.
- d2. LVIC temperature exceeds over temperature trip level (OT<sub>t</sub>).
- d3. IGBT OFF in spite of control input condition.
- d4. F<sub>o</sub> outputs during over temperature period, however, the minimum pulse width is 20μs.
- d5. LVIC temperature becomes under over temperature reset level.
- d6. Circuits start to operate normally when next input is applied.

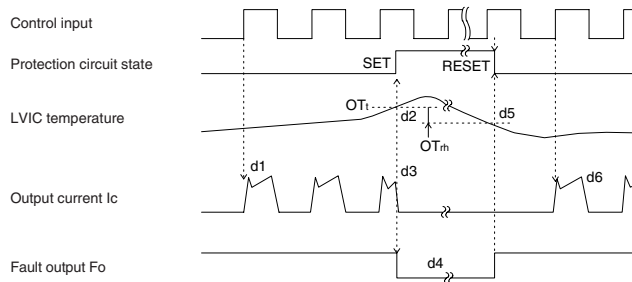
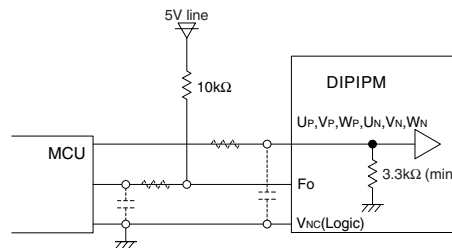


Fig. 9 RECOMMENDED MCU I/O INTERFACE CIRCUIT



**Note :** The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.  
The DIPIPM input section integrates a 3.3kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

Fig. 10 WIRING CONNECTION OF SHUNT RESISTOR

