



# 24AA00/24LC00/24C00

## 128-Bit I<sup>2</sup>C™ Bus Serial EEPROM

### Device Selection Table

Device	Vcc Range	Temp Range
24AA00	1.7-5.5	I
24LC00	2.5-5.5	I
24C00	4.5-5.5	I,E

### Features:

- Single supply with operation down to 1.7V for 24AA00 devices, 2.5V for 24LC00 devices
- Low-power CMOS technology:
  - Read current 500  $\mu$ A, typical
  - Standby current 100 nA, typical
- 2-wire serial interface, I<sup>2</sup>C™ compatible
- Schmitt Trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz and 400 kHz clock compatibility
- Page write time 3 ms, typical
- Self-timed erase/write cycle
- ESD protection >4000V
- More than 1 million erase/write cycles
- Data retention >200 years
- Factory programming available
- Packages include 8-lead PDIP, SOIC, TSSOP, DFN and 5-lead SOT-23
- Pb-free and RoHS compliant
- Temperature ranges available:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

### Description:

The Microchip Technology Inc. 24AA00/24LC00/24C00 (24XX00\*) is a 128-bit Electrically Erasable PROM memory organized as 16 x 8 with a 2-wire serial interface. Low-voltage design permits operation down to 1.7 volts for the 24AA00 version, and every version maintains a maximum standby current of only 1  $\mu$ A and typical active current of only 500  $\mu$ A. This device was designed for where a small amount of EEPROM is needed for the storage of calibration values, ID numbers or manufacturing information, etc. The 24XX00 is available in 8-pin PDIP, 8-pin SOIC (3.90 mm), 8-pin TSSOP, 8-pin 2x3 DFN and the 5-pin SOT-23 packages.

\*24XX00 is used in this document as a generic part number for the 24AA00/24LC00/24C00 devices.

### Package Types



### Block Diagram



### Pin Function Table

Name	Function
Vss	Ground
SDA	Serial Data
SCL	Serial Clock
Vcc	+1.7V to 5.5V (24AA00)
	+2.5V to 5.5V (24LC00)
	+4.5V to 5.5V (24C00)
NC	No Internal Connection

I<sup>2</sup>C is a trademark of Philips Corporation.

# 24AA00/24LC00/24C00

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings<sup>(†)</sup>

V <sub>CC</sub> .....	6.5V
All inputs and outputs w.r.t. V <sub>SS</sub> .....	-0.6V to V <sub>CC</sub> +1.0V
Storage temperature .....	-65°C to +150°C
Ambient temperature with power applied.....	-40°C to +125°C
ESD protection on all pins.....	4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

All Parameters apply across the recommended operating ranges unless otherwise noted	Industrial (I):	T <sub>A</sub> = -40°C to +85°C,		V <sub>CC</sub> = 1.8V to 5.5V	
	Automotive (E)	T <sub>A</sub> = -40°C to +125°C,		V <sub>CC</sub> = 4.5V to 5.5V	
Parameter	Symbol	Min.	Max.	Units	Conditions
SCL and SDA pins:					
High-level input voltage	V <sub>IH</sub>	0.7 V <sub>CC</sub>	—	V	<b>(Note)</b>
Low-level input voltage	V <sub>IL</sub>	—	0.3 V <sub>CC</sub>	V	<b>(Note)</b>
Hysteresis of Schmitt Trigger inputs	V <sub>HYS</sub>	.05 V <sub>CC</sub>	—	V	V <sub>CC</sub> ≥ 2.5V <b>(Note)</b>
Low-level output voltage	V <sub>OL</sub>	—	0.4	V	I <sub>OL</sub> = 3.0 mA, V <sub>CC</sub> = 4.5V I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 2.5V
Input leakage current	I <sub>LI</sub>	—	±1	μA	V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub>
Output leakage current	I <sub>LO</sub>	—	±1	μA	V <sub>OUT</sub> = V <sub>CC</sub> or V <sub>SS</sub>
Pin capacitance (all inputs/outputs)	C <sub>IN</sub> , C <sub>OUT</sub>	—	10	pF	V <sub>CC</sub> = 5.0V <b>(Note)</b> T <sub>A</sub> = 25°C, F <sub>CLK</sub> = 1 MHz
Operating current	I <sub>CC</sub> Write	—	2	mA	V <sub>CC</sub> = 5.5V, SCL = 400 kHz
	I <sub>CC</sub> Read	—	1	mA	V <sub>CC</sub> = 5.5V, SCL = 400 kHz
Standby current	I <sub>CCS</sub>	—	1	μA	V <sub>CC</sub> = 5.5V, SDA = SCL = V <sub>CC</sub>

**Note:** This parameter is periodically sampled and not 100% tested.

**FIGURE 1-1: BUS TIMING DATA**



**TABLE 1-2: AC CHARACTERISTICS**

All Parameters apply across all recommended operating ranges unless otherwise noted		Industrial (I): TA = -40°C to +85°C, VCC = 1.8V to 5.5V Automotive (E): TA = -40°C to +125°C, VCC = 4.5V to 5.5V			
Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK	— — —	100 100 400	kHz	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
Clock high time	THIGH	4000 4000 600	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
Clock low time	TLOW	4700 4700 1300	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
SDA and SCL rise time (Note 1)	TR	— — —	1000 1000 300	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
SDA and SCL fall time	TF	—	300	ns	(Note 1)
Start condition hold time	THD:STA	4000 4000 600	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
Start condition setup time	TSU:STA	4700 4700 600	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
Data input hold time	THD:DAT	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250 250 100	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
Stop condition setup time	TSU:STO	4000 4000 600	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
Output valid from clock (Note 2)	TAA	— — —	3500 3500 900	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
Bus free time: Time the bus must be free before a new transmission can start	TBUF	4700 4700 1300	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V
Output fall time from VIH minimum to VIL maximum	TOF	20+0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Notes 1, 3)
Write cycle time	TWC	—	4	ms	
Endurance		1M	—	cycles	(Note 4)

**Note 1:** Not 100% tested. CB = total capacitance of one bus line in pF.

- 2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
- 3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.
- 4:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained at [www.microchip.com](http://www.microchip.com).