

CD405xB CMOS Single 8-Channel Analog Multiplexer/Demultiplexer With Logic-Level Conversion

1 Features

- Wide Range of Digital and Analog Signal Levels
 - Digital: 3 V to 20 V
 - Analog: $\leq 20 V_{P-P}$
- Low ON Resistance, 125 Ω (Typical) Over 15 V_{P-P} Signal Input Range for $V_{DD} - V_{EE} = 18 V$
- High OFF Resistance, Channel Leakage of $\pm 100 pA$ (Typical) at $V_{DD} - V_{EE} = 18 V$
- Logic-Level Conversion for Digital Addressing Signals of 3 V to 20 V ($V_{DD} - V_{SS} = 3 V$ to 20 V) to Switch Analog Signals to 20 V_{P-P} ($V_{DD} - V_{EE} = 20 V$) Matched Switch Characteristics, $r_{ON} = 5 \Omega$ (Typical) for $V_{DD} - V_{EE} = 15 V$ Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2 μW (Typical) at $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10 V$
- Binary Address Decoding on Chip
- 5 V, 10 V, and 15 V Parametric Ratings
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1 μA at 18 V Over Full Package Temperature Range, 100 nA at 18 V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

2 Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating
- Factory Automation
- Televisions
- Appliances
- Consumer Audio
- Programmable Logic Circuits
- Sensors

3 Description

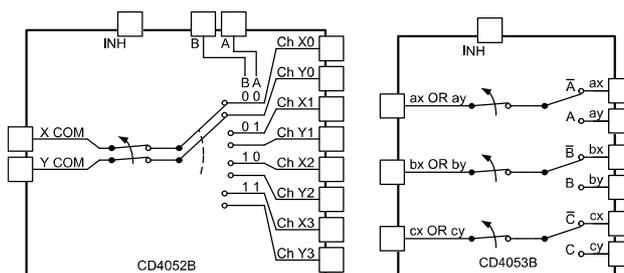
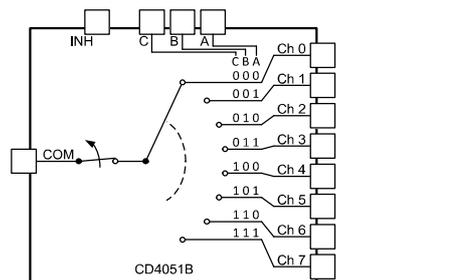
The CD405xB analog multiplexers and demultiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD405xB	CDIP (16)	19.50 mm × 6.92 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SOIC (16)	9.90 mm × 3.91 mm
	SOP (16)	10.30 mm × 5.30 mm
	TSSOP (16)	5.00 mm × 4.40 mm

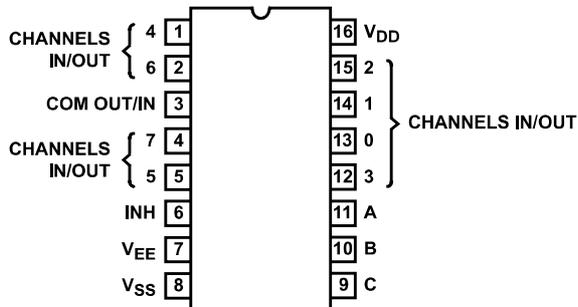
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagrams of CD405xB

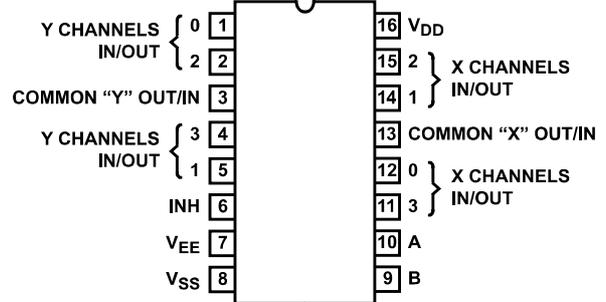


5 Pin Configuration and Functions

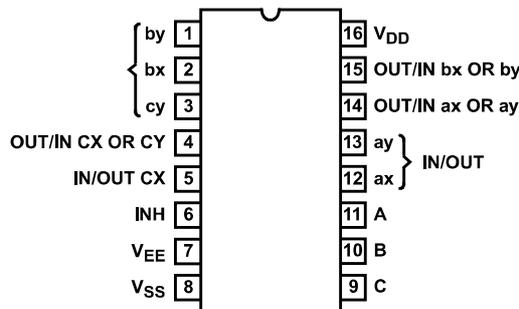
CD4051B E, M, NS, and PW Package
16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP
(Top View)



CD4052B E, M, NS, and PW Package
16-Pin PDIP, CDIP, SOP, and TSSOP
(Top View)



CD4053B E, M, NS, and PW Package
16-Pin PDIP, CDIP, SOP, and TSSOP
(Top View)



Pin Functions CD4051B

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CH 4 IN/OUT	I/O	Channel 4 in/out
2	CH 6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH 7 IN/OUT	I/O	Channel 7 in/out
5	CH 5 IN/OUT	I/O	Channel 5 in/out
6	INH	I	Disables all channels. See Table 1 .
7	V _{EE}	—	Negative power input
8	V _{SS}	—	Ground
9	C	I	Channel select C. See Table 1 .
10	B	I	Channel select B. See Table 1 .
11	A	I	Channel select A. See Table 1 .
12	CH 3 IN/OUT	I/O	Channel 3 in/out
13	CH 0 IN/OUT	I/O	Channel 0 in/out
14	CH 1 IN/OUT	I/O	Channel 1 in/out
15	CH 2 IN/OUT	I/O	Channel 2 in/out
16	V _{DD}	—	Positive power input

CD4051B, CD4052B, CD4053B

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Pin Functions CD4052B

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Y CH 0 IN/OUT	I/O	Channel Y0 in/out
2	Y CH 2 IN/OUT	I/O	Channel Y2 in/out
3	Y COM OUT/IN	I/O	Y common out/in
4	Y CH 3 IN/OUT	I/O	Channel Y3 in/out
5	Y CH 1 IN/OUT	I/O	Channel Y1 in/out
6	INH	I	Disables all channels. See Table 1 .
7	V _{EE}	—	Negative power input
8	V _{SS}	—	Ground
9	B	I	Channel select B. See Table 1 .
10	A	I	Channel select A. See Table 1 .
11	X CH 3 IN/OUT	I/O	Channel X3 in/out
12	X CH 0 IN/OUT	I/O	Channel X0 in/out
13	X COM IN/OUT	I/O	X common out/in
14	X CH 1 IN/OUT	I/O	Channel in/out
15	X CH 2 IN/OUT	I/O	Channel in/out
16	V _{DD}	—	Positive power input

Pin Functions CD4053B

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BY IN/OUT	I/O	B channel Y in/out
2	BX IN/OUT	I/O	B channel X in/out
3	CY IN/OUT	I/O	C channel Y in/out
4	CX OR CY OUT/IN	I/O	C common out/in
5	CX IN/OUT	I/O	C channel X in/out
6	INH	I	Disables all channels. See Table 1 .
7	V _{EE}	—	Negative power input
8	V _{SS}	—	Ground
9	C	I	Channel select C. See Table 1 .
10	B	I	Channel select B. See Table 1 .
11	A	I	Channel select A. See Table 1 .
12	AX IN/OUT	I/O	A channel X in/out
13	AY IN/OUT	I/O	A channel Y in/out
14	AX OR AY OUT/IN	I/O	A common out/in
15	BX OR BY OUT/IN	I/O	B common out/in
16	V _{DD}	—	Positive power input