

CD4553

3-Digit BCD Counter

The MC14553B 3-digit BCD counter consists of 3 negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Compatible Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

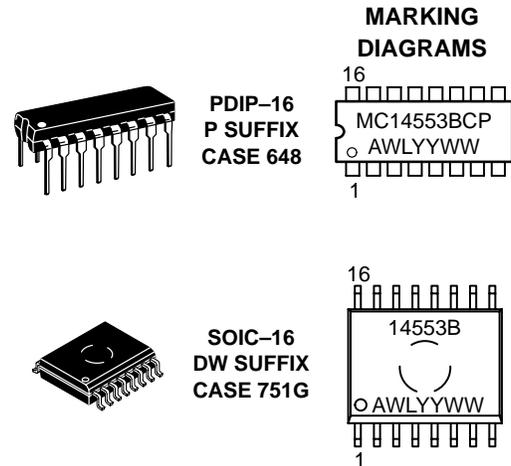
MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient) per Pin	± 10	mA
I_{out}	Output Current (DC or Transient) per Pin	+20	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	-55 to +125	$^{\circ}C$
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14553BCP	PDIP-16	25/Rail
MC14553BDW	SOIC-16	47/Rail

MC14553B

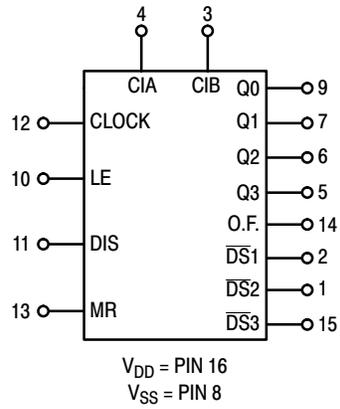


Figure 1. Block Diagram

TRUTH TABLE

Inputs				Outputs
Master Reset	Clock	Disable	LE	
0		0	0	No Change
0		0	0	Advance
0	X	1	X	No Change
0	1		0	Advance
0	1		0	No Change
0	0	X	X	No Change
0	X	X		Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don't Care

MC14553B

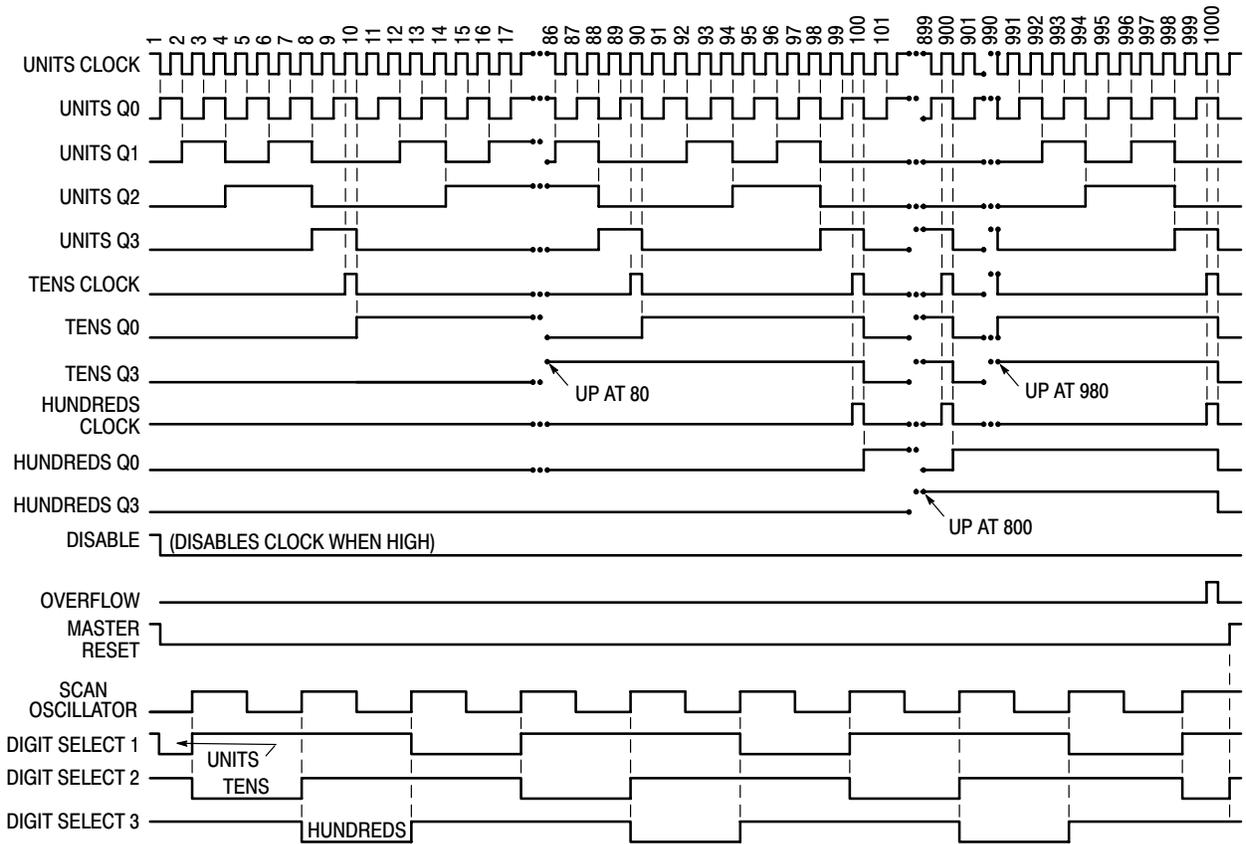


Figure 2. 3-Digit Counter Timing Diagram (Reference Figure 4)

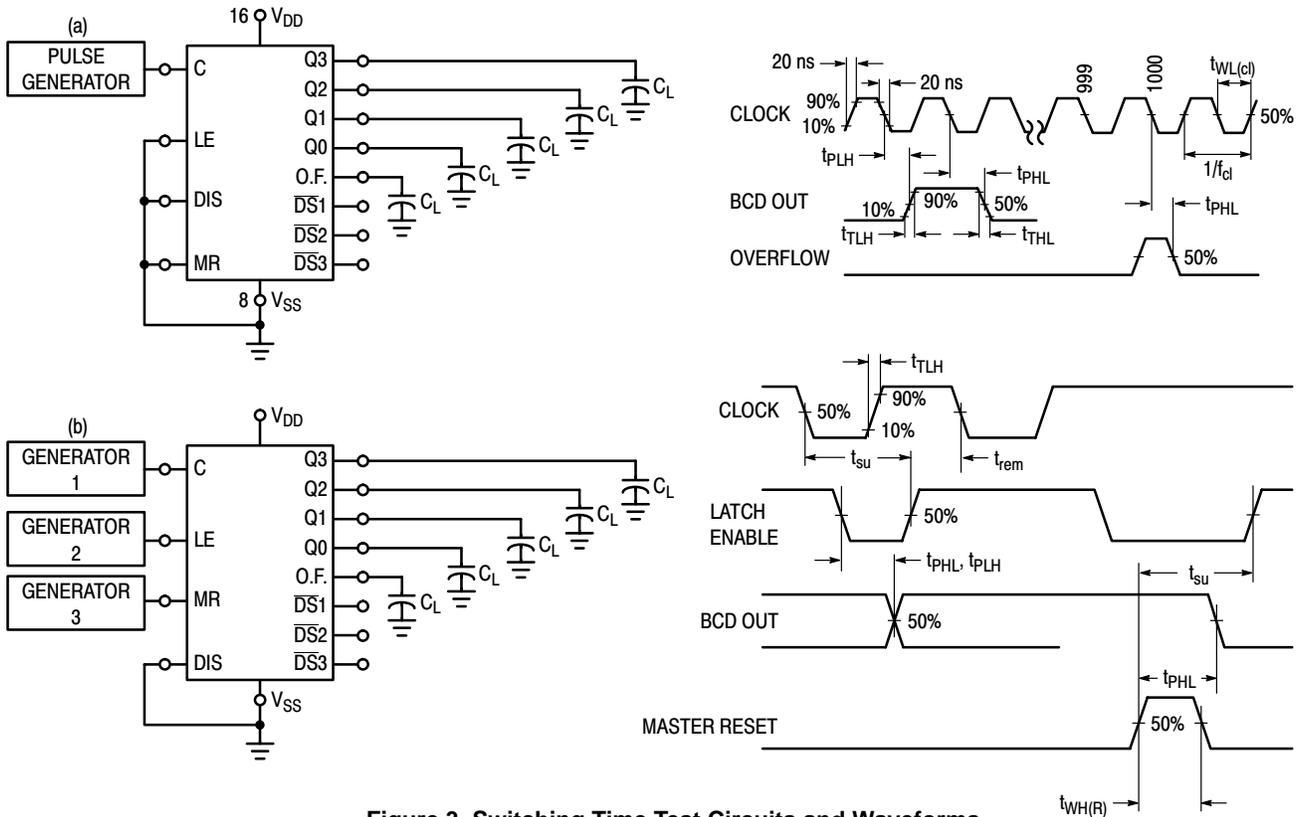


Figure 3. Switching Time Test Circuits and Waveforms