



DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to \overline{CP}) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

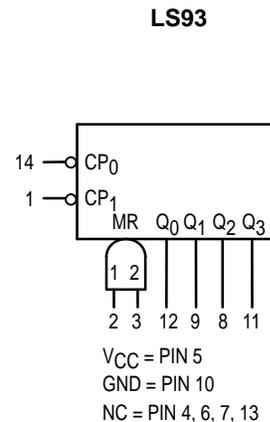
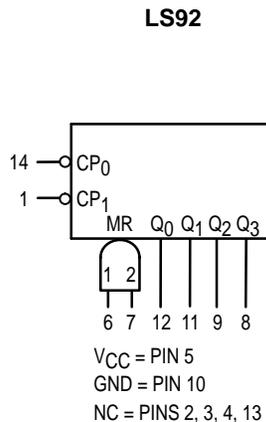
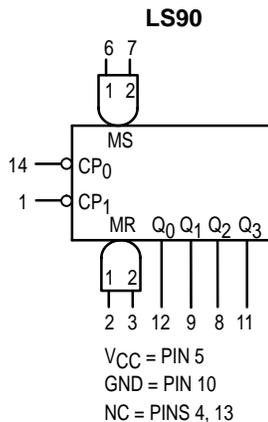
PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
\overline{CP}_0	Clock (Active LOW going edge) Input to +2 Section	0.5 U.L.	1.5 U.L.
\overline{CP}_1	Clock (Active LOW going edge) Input to +5 Section (LS90), +6 Section (LS92)	0.5 U.L.	2.0 U.L.
\overline{CP}_1	Clock (Active LOW going edge) Input to +8 Section (LS93)	0.5 U.L.	1.0 U.L.
MR ₁ , MR ₂	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS ₁ , MS ₂	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q ₀	Output from +2 Section (Notes b & c)	10 U.L.	5 (2.5) U.L.
Q ₁ , Q ₂ , Q ₃	Outputs from +5 (LS90), +6 (LS92), +8 (LS93) Sections (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:

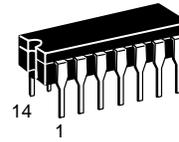
- 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
- The Q₀ Outputs are guaranteed to drive the full fan-out plus the \overline{CP}_1 input of the device.
- To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.

LOGIC SYMBOL

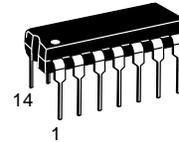


**SN54/74LS90
SN54/74LS92
SN54/74LS93**

**DECADE COUNTER;
DIVIDE-BY-TWELVE COUNTER;
4-BIT BINARY COUNTER
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



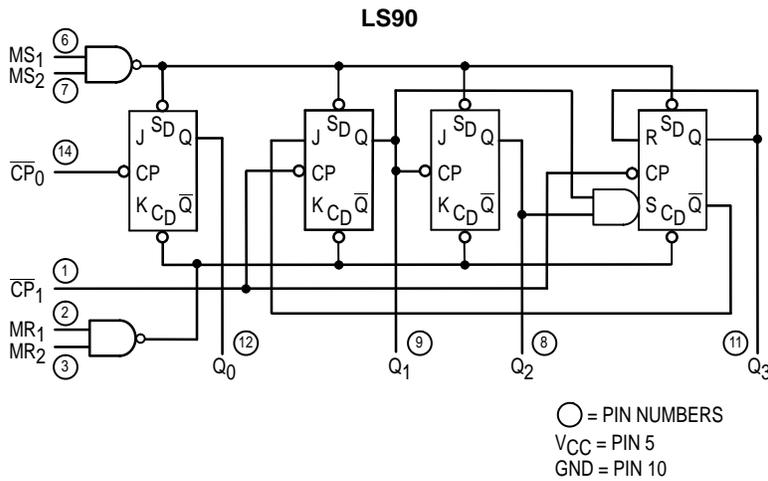
**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

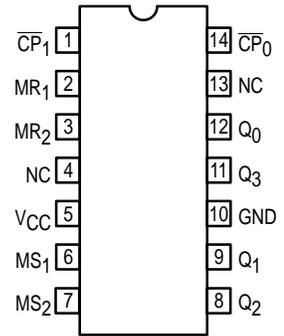
SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

SN54/74LS90 • SN54/74LS92 • SN54/74LS93

LOGIC DIAGRAM



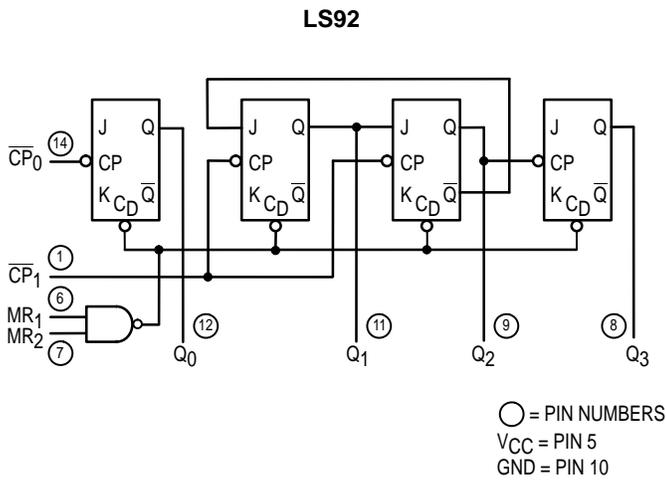
CONNECTION DIAGRAM DIP (TOP VIEW)



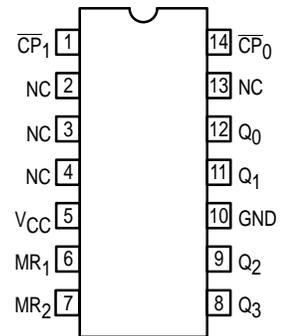
NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



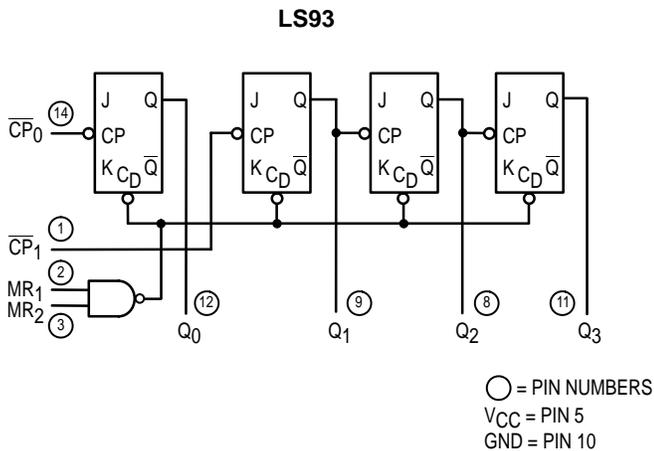
CONNECTION DIAGRAM DIP (TOP VIEW)



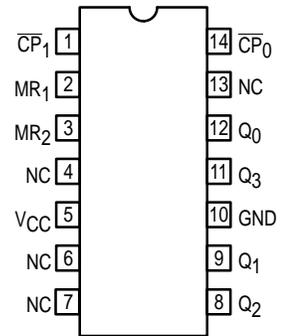
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LOGIC DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

NOTE:
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SN54/74LS90 • SN54/74LS92 • SN54/74LS93

FUNCTIONAL DESCRIPTION

The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the \overline{CP}_1 input of the device.

A gated AND asynchronous Master Reset ($MR_1 \bullet MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \bullet MS_2$) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

- A. BCD Decade (8421) Counter — The \overline{CP}_1 input must be externally connected to the Q_0 output. The \overline{CP}_0 input receives the incoming count and a BCD count sequence is produced.
- B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the \overline{CP}_0 input. The input count is then applied to the \overline{CP}_1 input and a divide-by-ten square wave is obtained at output Q_0 .

- C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

- A. Modulo 12, Divide-By-Twelve Counter — The \overline{CP}_1 input must be externally connected to the Q_0 output. The \overline{CP}_0 input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.
- B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The \overline{CP}_1 input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

LS93

- A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input \overline{CP}_1 . The input count pulses are applied to input \overline{CP}_0 . Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0 , Q_1 , Q_2 , and Q_3 outputs as shown in the truth table.
- B. 3-Bit Ripple Counter — The input count pulses are applied to input \overline{CP}_1 . Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1 , Q_2 , and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.