TEA1755T

HV start-up DCM/QR flyback controller with integrated DCM/QR PFC controller

Rev. 1.1 — 13 March 2015 Product data sheet

1. General description

The GreenChip is the latest generation of green Switched Mode Power Supply (SMPS) controller ICs. The TEA1755T combines a controller for Power Factor Correction (PFC) and a flyback controller. Its high level of integration enables cost-effective power supply design using a very low number of external components.

The PFC operates in Quasi-Resonant (QR) or Discontinuous Conduction Mode (DCM), with valley switching.

The specially built-in green functions provide high efficiency at all power levels. At high power levels the flyback operates in QR mode or DCM with valley detection. At medium power levels, the flyback controller switches to Frequency Reduction (FR) mode and limits the peak current to an adjustable minimum value. In low power mode, the PFC switches off to maintain high efficiency. At very low power levels, when the flyback switching frequency drops below 25 kHz, the flyback converter switches to burst mode. During the non-switching phase of burst mode, the internal IC supply current is minimized to further optimize efficiency. Valley switching is used in all operating modes.

The advanced burst mode ensures high-efficiency at low power and good standby power performance while minimizing audible transformer noise.

The TEA1755T is a Multi-Chip Module, (MCM), containing two chips. The proprietary high-voltage BCD800 process makes direct start-up possible from the rectified universal mains voltage in an effective and green way. The second low voltage Silicon-On-Insulator (SOI) is used for accurate, high-speed protection functions and control.

The TEA1755T enables easy design of highly efficient and reliable supplies up to 250 W. These power supply designs are cost-effective, requiring the minimum number of external components.

Remark: All values in this document are typical values unless otherwise stated.

2. Features and benefits

2.1 Distinctive features

- Integrated PFC and flyback controller
- Universal mains supply operation between 70 V (AC) to 276 V (AC)
- Dual-boost PFC with accurate maximum output voltage (NXP Semiconductors patented)
- High level of integration, results in cost-effective designs with very low external component counts
- Adjustable PFC switch off delay
- External PFC switch on and switch off override
- Accurate PFC switch on and switch off control (NXP Semiconductors patent pending)

2.2 Green features

- On-chip start-up current source
- Reduced IC supply current during burst mode enabling ErP lot 6
- Power-down functionality for very low standby power

2.3 PFC green features

- Valley/Zero-Voltage Switching (ZVS) for minimum switching losses (NXP Semiconductors patented)
- Frequency limitation reduces switching losses
- PFC switched off when a low-load is detected at the flyback output

2.4 Flyback green features

- Valley switching for minimum switching losses (NXP Semiconductors patented)
- Frequency reduction with adjustable minimum peak current at low-power operation maintains high-efficiency at low output power levels
- Burst mode operation at very low-power levels for high-efficiency operation

2.5 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection using demagnetization detection for both converters (NXP Semiconductors patented)
- UnderVoltage Protection (UVP) (foldback during overload)
- Accurate OverVoltage Protection (OVP) for both converters (adjustable for flyback converter)
- Mains voltage independent OverPower Protection (OPP)
- Open control loop protection for both converters. The open-loop protection on the flyback converter is safe restart
- OverTemperature Protection (OTP)
- Low and adjustable OverCurrent Protection (OCP) trip level for both converters
- General-purpose input for latched protection, for use with system OverTemperature Protection (OTP)

3. Applications

- The device can be used in all applications requiring an efficient and cost-effective power supply solution for up to 250 W. Notebook adapters in particular benefit from the high level of integration

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1755T/1	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Block diagram

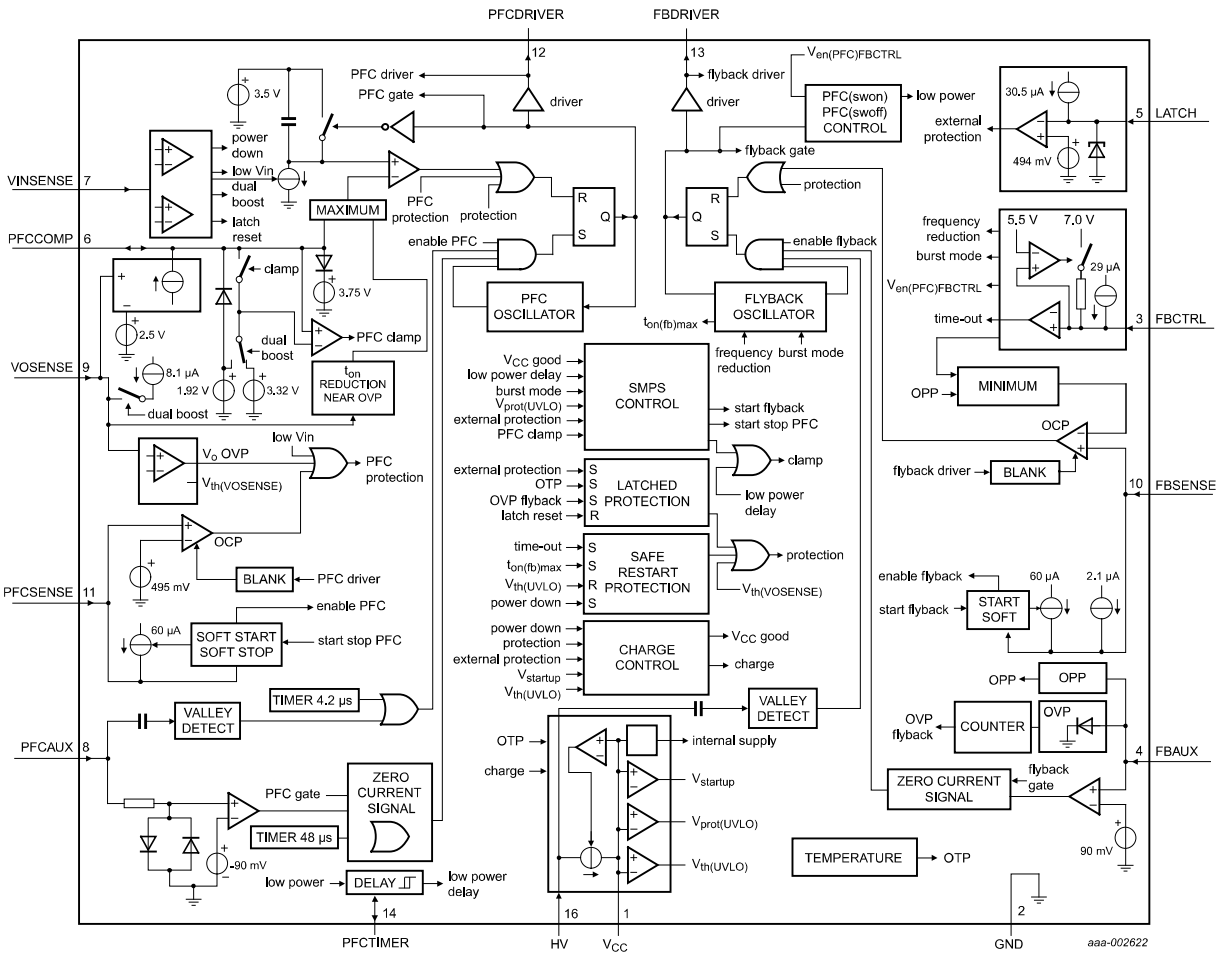


Fig 1. TEA1755T block diagram

6. Pinning information

6.1 Pinning

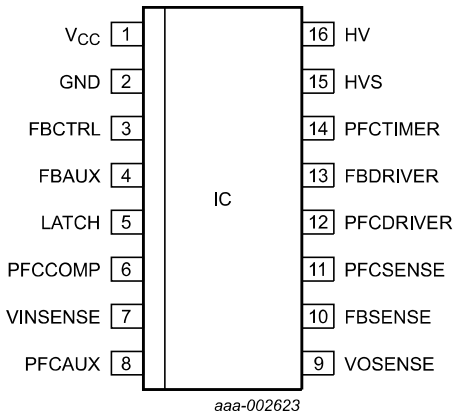


Fig 2. TEA1755T pin configuration (SOT109-1)

6.2 Pin description

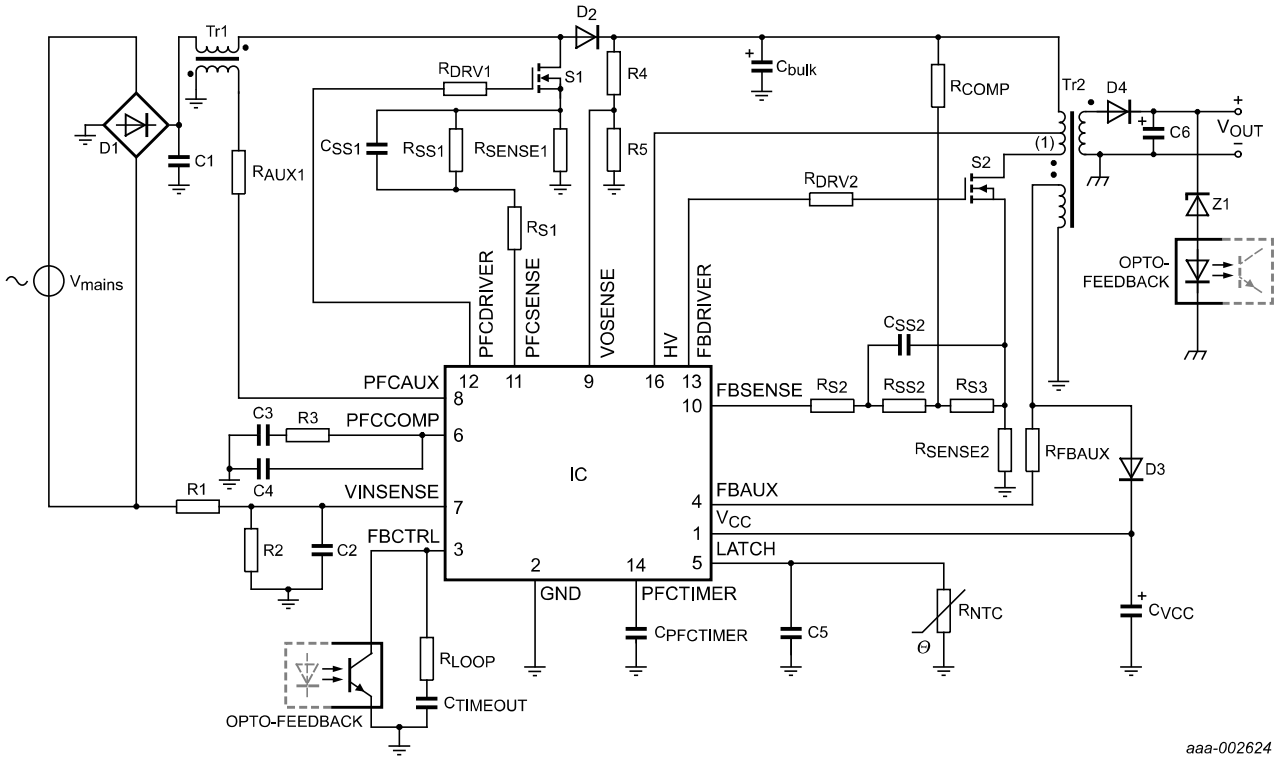
Table 2. Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
GND	2	ground
FBCTRL	3	flyback control input
FBAUX	4	auxiliary winding input for demagnetization timing and flyback OVP
LATCH	5	general-purpose protection input
PFCCOMP	6	PFC frequency compensation
VINSENSE	7	mains voltage sense input
PFCAUX	8	auxiliary winding input for demagnetization timing of the PFC
VOSENSE	9	sense input for PFC output voltage
FBSENSE	10	flyback current sense input
PFCSENSE	11	PFC current sense input
PFCDRIVER	12	PFC gate-driver output
FBDRIVER	13	flyback gate-driver output
PFCTIMER	14	PFC override and switch off delay timer
HVS	15	high-voltage safety spacer; not connected
HV	16	high-voltage start-up and flyback valley sensing

7. Functional description

7.1 General control

The TEA1755T contains a power factor correction circuit controller and a flyback circuit controller. A typical configuration is shown in Figure 3.



(1) The HV pin can either be connected to the center tap of the flyback transformer or to the drain of MOSFET S2.

Fig 3. A typical TEA1755T configuration

7.1.1 Start-up and UnderVoltage LockOut (UVLO)

Initially, the capacitor on the V_{CC} pin is charged from the high-voltage mains using the HV pin.

When V_{CC} is less than V_{trip}, the charge current is $I_{ch(low)}$. This low current protects the IC if the V_{CC} pin is shorted to ground. To ensure a short start-up time, the charge current above the V_{trip} level is increased to $I_{ch(high)}$, until V_{CC} reaches $V_{th(UVLO)}$. When V_{CC} is between $V_{th(UVLO)}$ and $V_{startup}$, the charge current goes low again to ensure a low safe restart duty cycle during fault conditions.

The control logic activates the internal circuitry and switches off the HV charge current when V_{CC} passes the $V_{startup}$ level. First, the LATCH pin current source is activated and the soft-start capacitors on the PFCSENSE and FBSENSE pins are charged. Also the clamp circuit on the PFCCOMP pin is activated.

The PFC circuit is activated when the following conditions are met: