TPA3110D2 15-W Fil ter-Free Stereo Class-D Audio Power Amplifier With Speakerguard™

1 Features

- 15-W/ch into an 8-Ω Loads at 10% THD+N From a 16-V Supply
- 10-W/ch into 8-Ω Loads at 10% THD+N From a 13-V Supply
- 30-W into a 4-Ω Mono Load at 10% THD+N From a 16-V Supply
- 90% Efficient Class-D Operation Eliminates Need for Heat Sinks
- Wide Supply Voltage Range Allows Operation From 8 V to 26 V
- Filter-Free Operation
- SpeakerGuard™ Speaker Protection Includes Adjustable Power Limiter Plus DC Protection
- Flow Through Pin Out Facilitates Easy Board Layout
- Robust Pin-to-Pin Short Circuit Protection and Thermal Protection With Auto Recovery Option
- Excellent THD+N / Pop-Free Performance
- Four Selectable, Fixed Gain Settings
- Differential Inputs

2 Applications

- Televisions
- Consumer Audio Equipment

3 Description

The TPA3110D2 is a 15-W (per channel) efficient, Class-D audio power amplifier for driving bridged-tied stereo speakers. Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard™ speaker protection circuitry includes an adjustable power limiter and a DC detection circuit. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detect circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs.

The TPA3110D2 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3110D2, 90%, eliminates the need for an external heat sink when playing music.

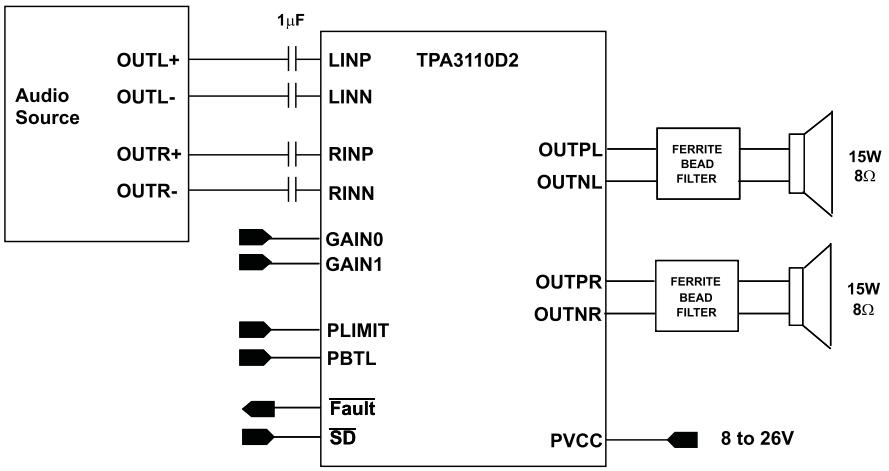
The outputs are also fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA3110D2	HTSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPA3110D2 Simplified Application Schematic



5 Device Comparison Table

DEVICE NUMBER	SPEAKER CHANNELS	SPEAKER AMP TYPE	OUTPUT POWER (W)	ADDITIONAL FEATURES
TPA3110D2	Stereo	Class D	15	Power limiter
TPA3130D1	Stereo	Class D	15	
TPA3118D2	Stereo	Class D	30	Power limiter
TPA3116D1	Stereo	Class D	50	Power limiter

6 Pin Configuration and F unctions

PWP Package
28-Pin HTSSOP With PowerPAD™
Top View

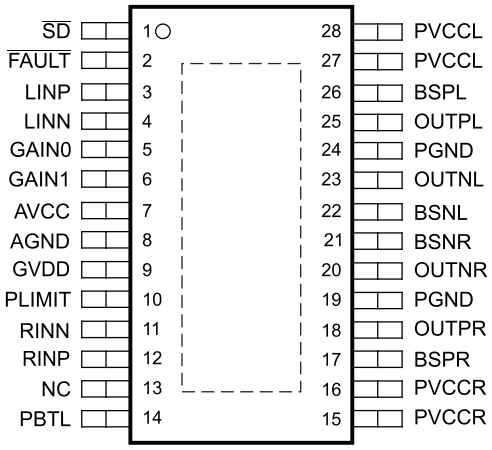


Table 1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{SD}$	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
2	$\overline{FAULT}$	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
3	LINP	I	Positive audio input for left channel. Biased at 3 V.
4	LINN	I	Negative audio input for left channel. Biased at 3 V.
5	GAIN0	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
6	GAIN1	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
7	AVCC	P	Analog supply
8	AGND	—	Analog signal ground. Connect to the thermal pad.
9	GVDD	O	High-side FET gate drive supply. Nominal voltage is 7V. Also should be used as supply for PLIMIT function.
10	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
11	RINN	I	Negative audio input for right channel. Biased at 3 V.
12	RINP	I	Positive audio input for right channel. Biased at 3 V.
13	NC	—	Not connected
14	PBTL	I	Parallel BTL mode switch

Table 1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
15	PVCCR	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
16	PVCCR	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
17	BSPR	I	Bootstrap I/O for right channel, positive high-side FET.
18	OUTPR	O	Class-D H-bridge positive output for right channel.
19	PGND	—	Power ground for the H-bridges.
20	OUTNR	O	Class-D H-bridge negative output for right channel.
21	BSNR	I	Bootstrap I/O for right channel, negative high-side FET.
22	BSNL	I	Bootstrap I/O for left channel, negative high-side FET.
23	OUTNL	O	Class-D H-bridge negative output for left channel.
24	PGND	—	Power ground for the H-bridges.
25	OUTPL	O	Class-D H-bridge positive output for left channel.
26	BSPL	I	Bootstrap I/O for left channel, positive high-side FET.
27	PVCCL	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.
28	PVCCL	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3 V	30 V	V
V_I	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, $\overline{FAULT}$ (2)	–0.3 V	V_{CC} + 0.3 V	V
				< 10 V/ms	
		PLIMIT	–0.3	GVDD + 0.3	V
		RINN, RINP, LINN, LINP	–0.3	6.3	V
	Continuous total power dissipation		See *Thermal Information*		
R_L	Minimum Load Resistance	BTL: PVCC > 15 V		4.8	
		BTL: PVCC ≤ 15 V		3.2	
		PBTL		3.2	
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature range(3)		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage slew rate of these pins must be restricted to no more than 10 V/ms. For higher slew rates, use a 100-kΩ resister in series with the pins.
(3) The TPA3110D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SLMA002 for more information about using the TSSOP thermal pad.