

TPA3116D2 15-W, 30-W, 50-W Filter-Free Class-D Stereo Amplifier Family With AM Avoidance

1 Features

- Supports Multiple Output Configurations
 - 2 × 50 W Into a 4-Ω BTL Load at 21 V (TPA3116D2)
 - 2 × 30 W Into a 8-Ω BTL Load at 24 V (TPA3118D2)
 - 2 × 15 W Into a 8-Ω BTL Load at 15 V (TPA3130D2)
- Wide Voltage Range: 4.5 V to 26 V
- Efficient Class-D Operation
 - >90% Power Efficiency Combined With Low Idle Loss Greatly Reduces Heat Sink Size
 - Advanced Modulation Schemes
- Multiple Switching Frequencies
 - AM Avoidance
 - Master and Slave Synchronization
 - Up to 1.2-MHz Switching Frequency
- Feedback Power-Stage Architecture With High PSRR Reduces PSU Requirements
- Programmable Power Limit
- Differential and Single-Ended Inputs
- Stereo and Mono Mode With Single-Filter Mono Configuration
- Single Power Supply Reduces Component Count
- Integrated Self-Protection Circuits Including Overvoltage, Undervoltage, Overtemperature, DC-Detect, and Short Circuit With Error Reporting
- Thermally Enhanced Packages
 - DAD (32-Pin HTSSOP Pad Up)
 - DAP (32-Pin HTSSOP Pad Down)
- –40°C to 85°C Ambient Temperature Range

2 Applications

- Mini-Micro Component, Speaker Bar, Docks
- After-Market Automotive
- CRT TV
- Consumer Audio Applications

3 Description

The TPA31xxD2 series are stereo efficient, digital amplifier power stage for driving speakers up to 100 W / 2 Ω in mono. The high efficiency of the TPA3130D2 allows it to do 2 × 15 W without external heat sink on a single layer PCB. The TPA3118D2 can even run 2 × 30 W / 8 Ω without heat sink on a dual layer PCB. If even higher power is needed the TPA3116D2 does 2 × 50 W / 4 Ω with a small heat-sink attached to its top side PowerPAD. All three devices share the same footprint enabling a single PCB to be used across different power levels.

The TPA31xxD2 advanced oscillator/PLL circuit employs a multiple switching frequency option to avoid AM interferences; this is achieved together with an option of either master or slave option, making it possible to synchronize multiple devices.

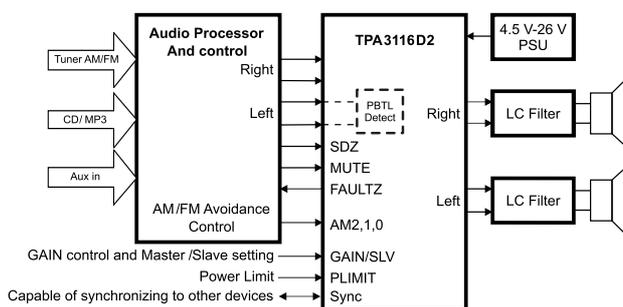
The TPA31xxD2 devices are fully protected against faults with short-circuit protection and thermal protection as well as overvoltage, undervoltage, and DC protection. Faults are reported back to the processor to prevent devices from being damaged during overload conditions.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA3116D2	DAD (32)	11.00 mm × 6.20 mm
TPA3118D2 TPA3130D2	DAP (32)	11.00 mm × 6.20 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Circuit

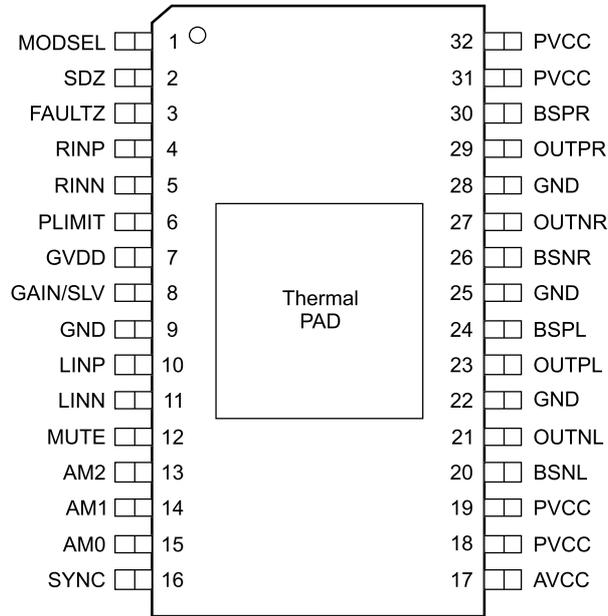


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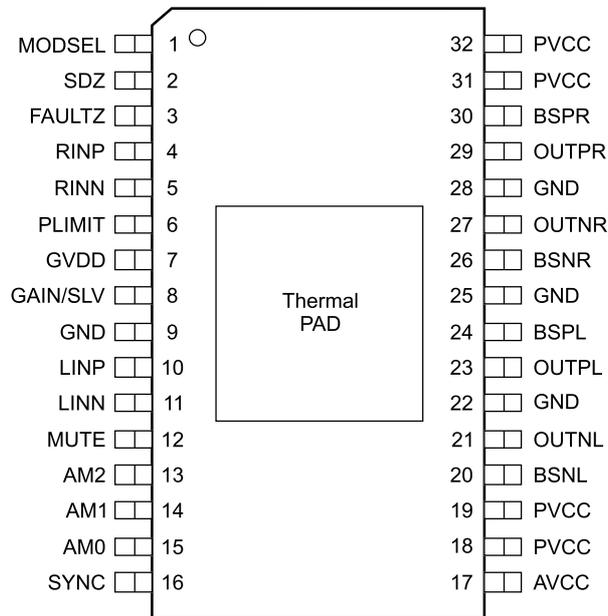


5 Pin Configuration and Functions

DAD Package
32-Pin HTSSOP With PowerPAD Up
TPA3116D2 Only, Top View



DAP Package
32-Pin HTSSOP With PowerPAD Down
Top View



TPA3116D2, TPA3118D2, TPA3130D2

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Pin Functions

NO.	PIN		TYPE ⁽¹⁾	DESCRIPTION
	NAME			
1	MODSEL	I		Mode selection logic input (LOW = BD mode, HIGH = 1 SPW mode). TTL logic levels with compliance to AVCC.
2	SDZ	I		Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
3	FAULTZ	DO		General fault reporting including Over-temp, DC Detect. Open drain. FAULTZ = High, normal operation FAULTZ = Low, fault condition
4	RINP	I		Positive audio input for right channel. Biased at 3 V.
5	RINN	I		Negative audio input for right channel. Biased at 3 V.
6	PLIMIT	I		Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
7	GVDD	PO		Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 μ F X7R ceramic decoupling capacitor and the PLIMIT and GAIN/SLV resistor dividers.
8	GAIN/SLV	I		Selects Gain and selects between Master and Slave mode depending on pin voltage divider.
9	GND	G		Ground
10	LINP	I		Positive audio input for left channel. Biased at 3 V. Connect to GND for PBTL mode.
11	LINN	I		Negative audio input for left channel. Biased at 3 V. Connect to GND for PBTL mode.
12	MUTE	I		Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
13	AM2	I		AM Avoidance Frequency Selection
14	AM1	I		AM Avoidance Frequency Selection
15	AM0	I		AM Avoidance Frequency Selection
16	SYNC	DIO		Clock input/output for synchronizing multiple class-D devices. Direction determined by GAIN/SLV terminal.
17	AVCC	P		Analog Supply
18	PVCC	P		Power supply
19	PVCC	P		Power supply
20	BSNL	BST		Boot strap for negative left channel output, connect to 220 nF X5R, or better ceramic cap to OUTNL
21	OUTNL	PO		Negative left channel output
22	GND	G		Ground
23	OUTPL	PO		Positive left channel output
24	BSPL	BST		Boot strap for positive left channel output, connect to 220 nF X5R, or better ceramic cap to OUTPL
25	GND	G		Ground
26	BSNR	BST		Boot strap for negative right channel output, connect to 220 nF X5R, or better ceramic cap to OUTNR
27	OUTNR	PO		Negative right channel output
28	GND	G		Ground
29	OUTPR	PO		Positive right channel output
30	BSPR	BST		Boot strap for positive right channel output, connect to 220 nF X5R or better ceramic cap to OUTPR
31	PVCC	P		Power supply
32	PVCC	P		Power supply
33	PowerPAD	G		Connect to GND for best system performance. If not connected to GND, leave floating.

(1) **TYPE:** DO = Digital Output, I = Analog Input, G = General Ground, PO = Power Output, BST = Boot Strap.