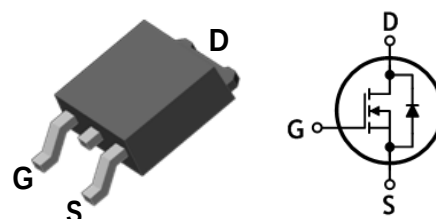


200V LOGIC N-Channel MOSFET

Features

- Drain-Source breakdown voltage: $BV_{DSS}=200V$ (Min.)
- Low gate charge: $Q_g=12nC$ (Typ.)
- Low drain-source On-Resistance: $R_{DS(on)}=0.34\Omega$ (Typ.)
- 100% avalanche tested
- RoHS compliant device

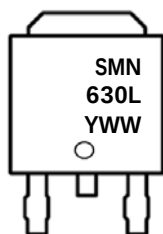


TO-252

Ordering Information

Part Number	Marking	Package
SMN630LD	SMN630L	TO-252

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW
 -. YWW: Date Code (year, week)

Absolute maximum ratings ($T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	200	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current (DC) *	I_D	$T_c=25^\circ C$	9 A
		$T_c=100^\circ C$	5.7 A
Drain current (Pulsed) *	I_{DM}	36	A
Avalanche current ^(Note 2)	I_{AS}	9	A
Single pulsed avalanche energy ^(Note 2)	E_{AS}	216	mJ
Repetitive avalanche current ^(Note 1)	I_{AR}	9	A
Repetitive avalanche energy ^(Note 1)	E_{AR}	4.5	mJ
Power dissipation	P_D	45	W
Junction temperature	T_J	150	$^\circ C$
Storage temperature range	T_{stg}	-55-150	$^\circ C$

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.77	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 50	

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	200	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	1	-	2.5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=200\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=4.5\text{A}$	-	0.34	0.4	Ω
		$V_{GS}=5\text{V}$, $I_D=4.5\text{A}$	-	0.37	0.44	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS}=10\text{V}$, $I_D=4.5\text{A}$	-	5.5	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	575	804	pF
Output capacitance	C_{oss}		-	84	112	
Reverse transfer capacitance	C_{rss}		-	10.5	15	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=100\text{V}$, $I_D=9\text{A}$ $R_G=25\Omega$	-	20	-	ns
Rise time (Note 3,4)	t_r		-	79	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	155	-	
Fall time (Note 3,4)	t_f		-	42	-	
Total gate charge (Note 3,4)	Q_g	$V_{DS}=160\text{V}$, $V_{GS}=10\text{V}$ $I_D=9\text{A}$	-	12	17	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	3	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	2	-	

Source-Drain Diode Ratings and Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	9	A
Source current (Pulsed)	I_{SM}		-	-	36	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=9\text{A}$	-	-	1.5	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=9\text{A}$, $V_{GS}=0\text{V}$ $di_S/dt=100\text{A}/\mu\text{s}$	-	125	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	0.5	-	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=4\text{mH}$, $I_{AS}=9\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycles $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Typical Characteristics Curves

Fig. 1 $I_D - V_{DS}$

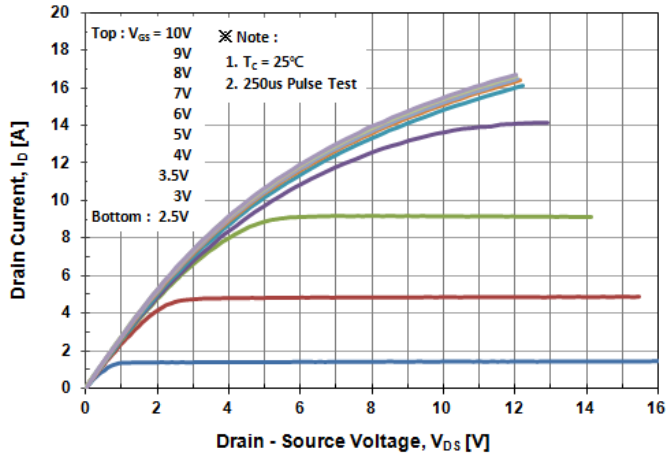


Fig. 2 $I_D - V_{GS}$

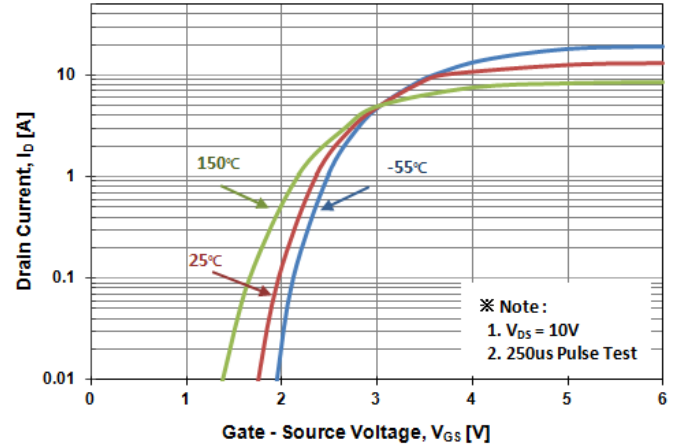


Fig. 3 $R_{DS(ON)} - I_D$

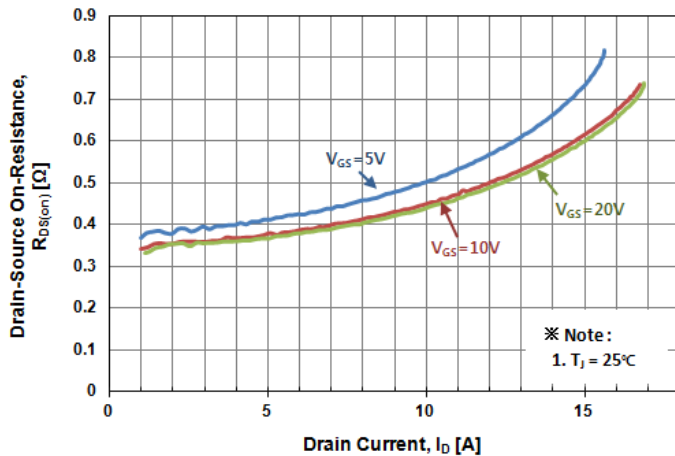


Fig. 4 $I_S - V_{SD}$

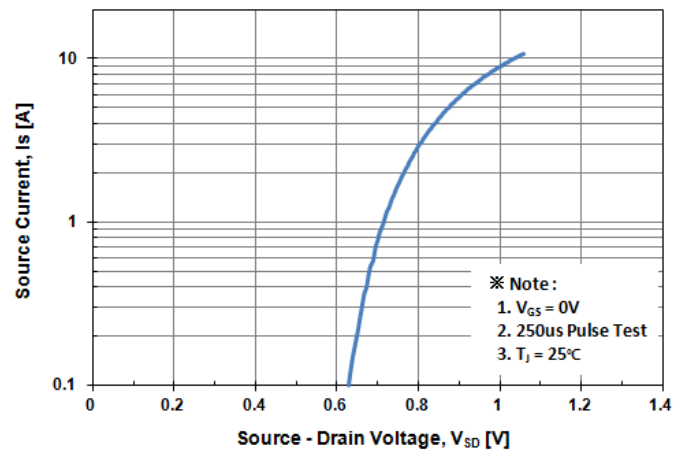


Fig. 5 Capacitance - V_{DS}

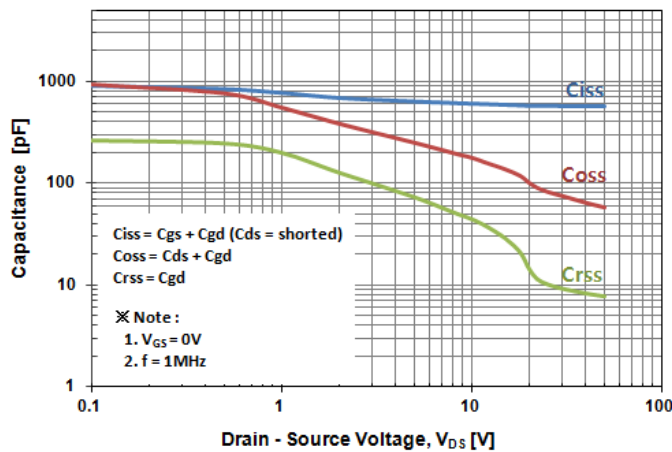


Fig. 6 $V_{GS} - Q_G$

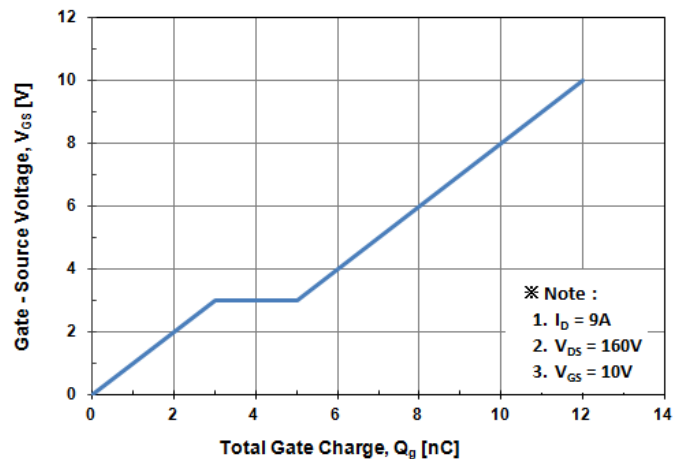


Fig. 7 $BV_{DSS} - T_J$

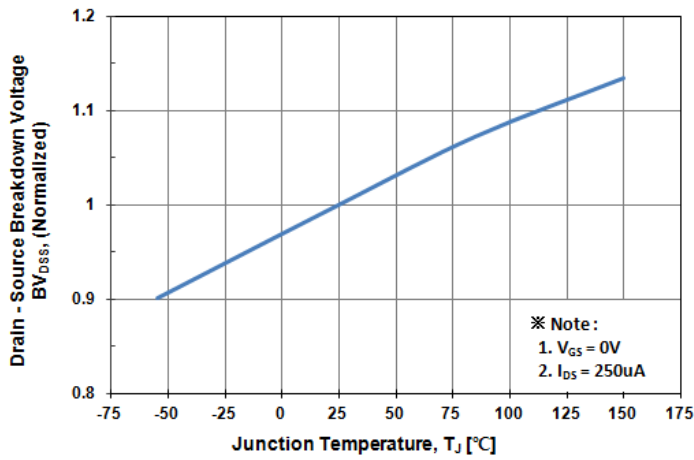


Fig. 8 $R_{DS(on)} - T_J$

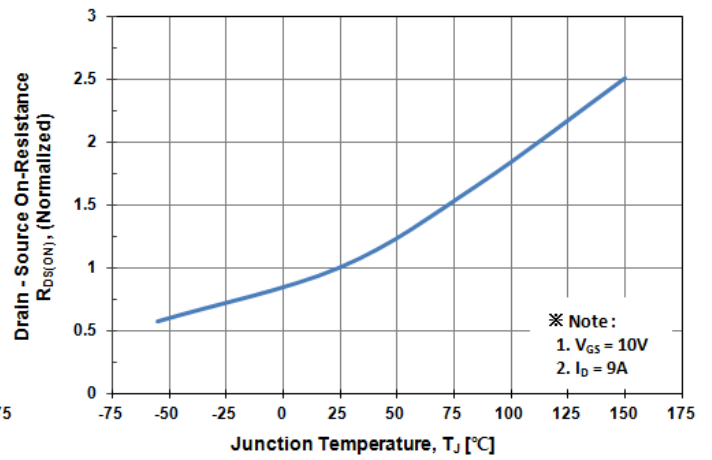


Fig. 9 $I_D - T_C$

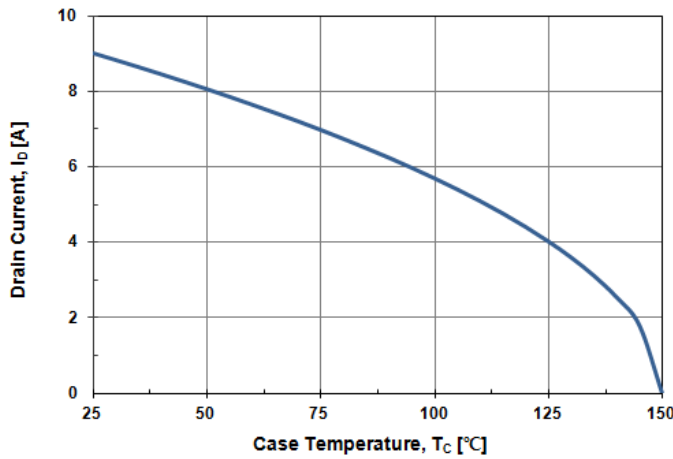


Fig. 10 Safe Operating Area

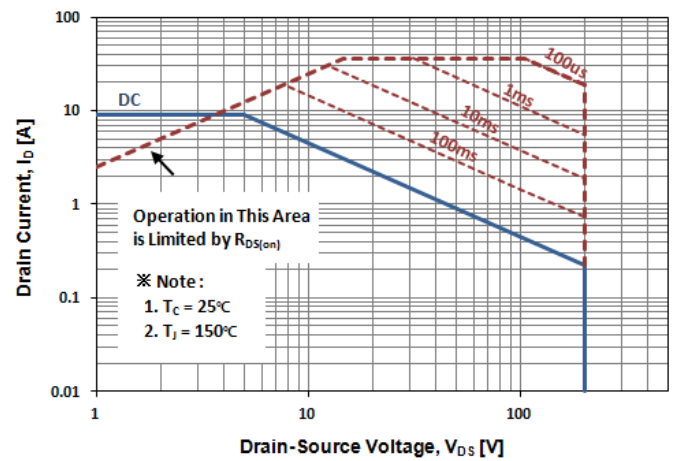


Fig. 11 Transient Thermal Impedance

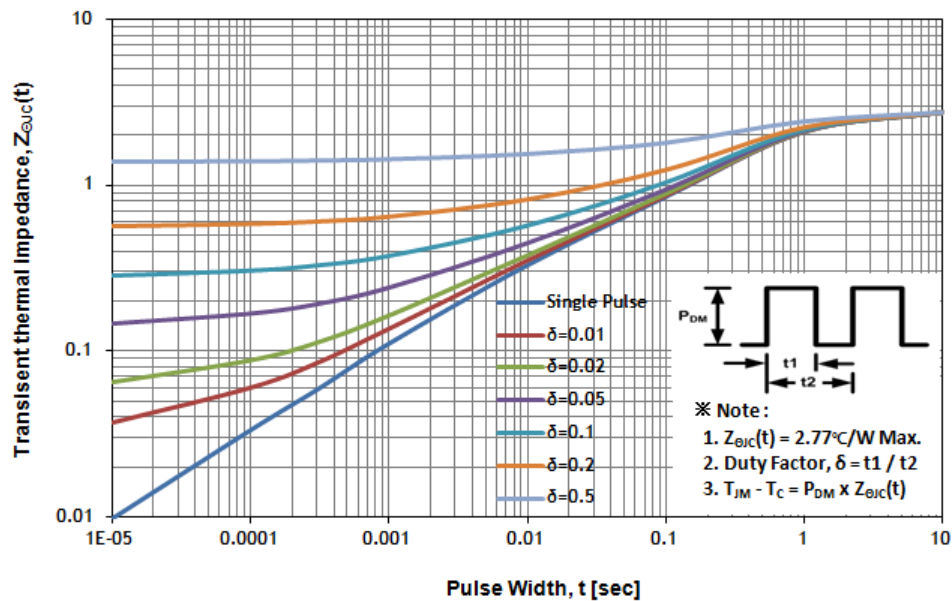


Fig. 12 Gate Charge Test Circuit & Waveform

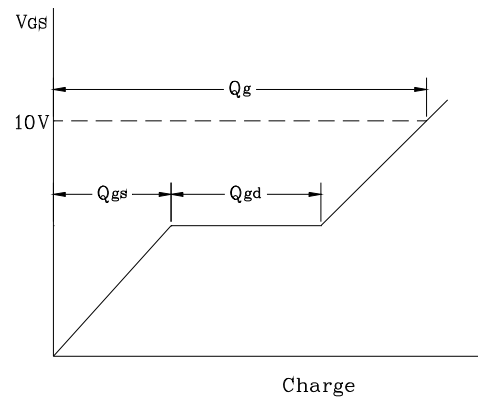
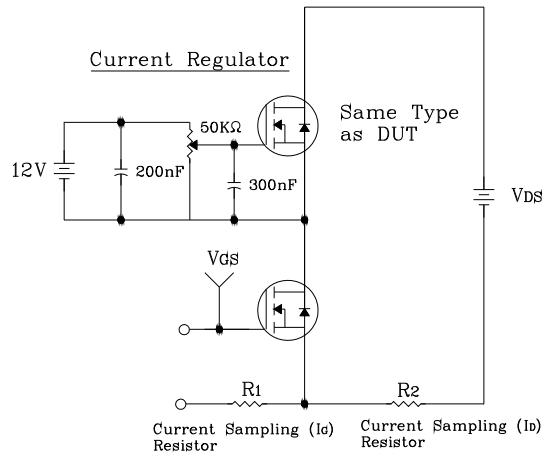


Fig. 13 Resistive Switching Test Circuit & Waveform

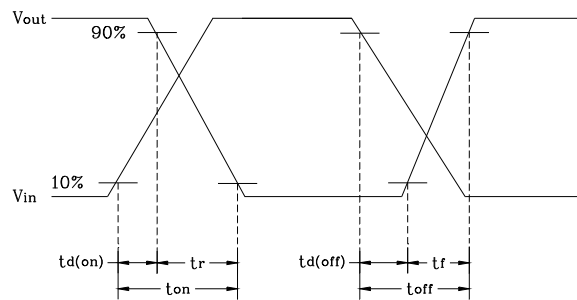
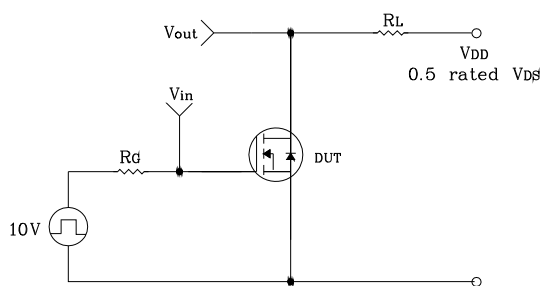


Fig. 14 E_{AS} Test Circuit & Waveform

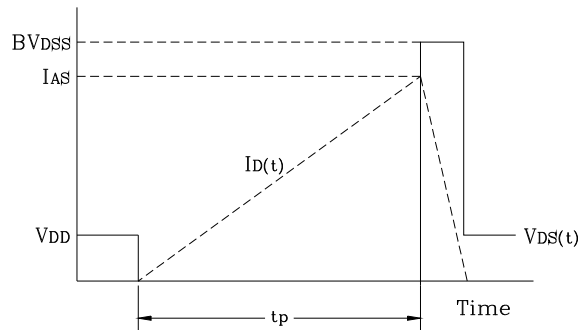
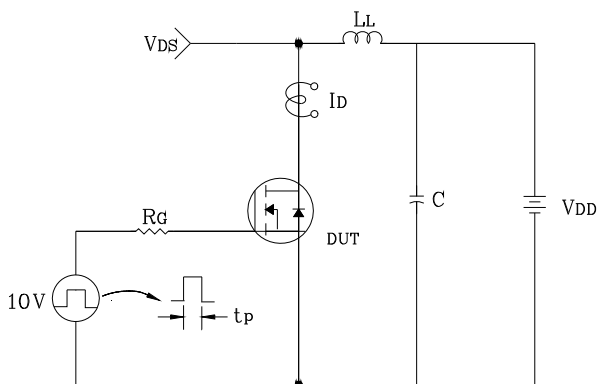
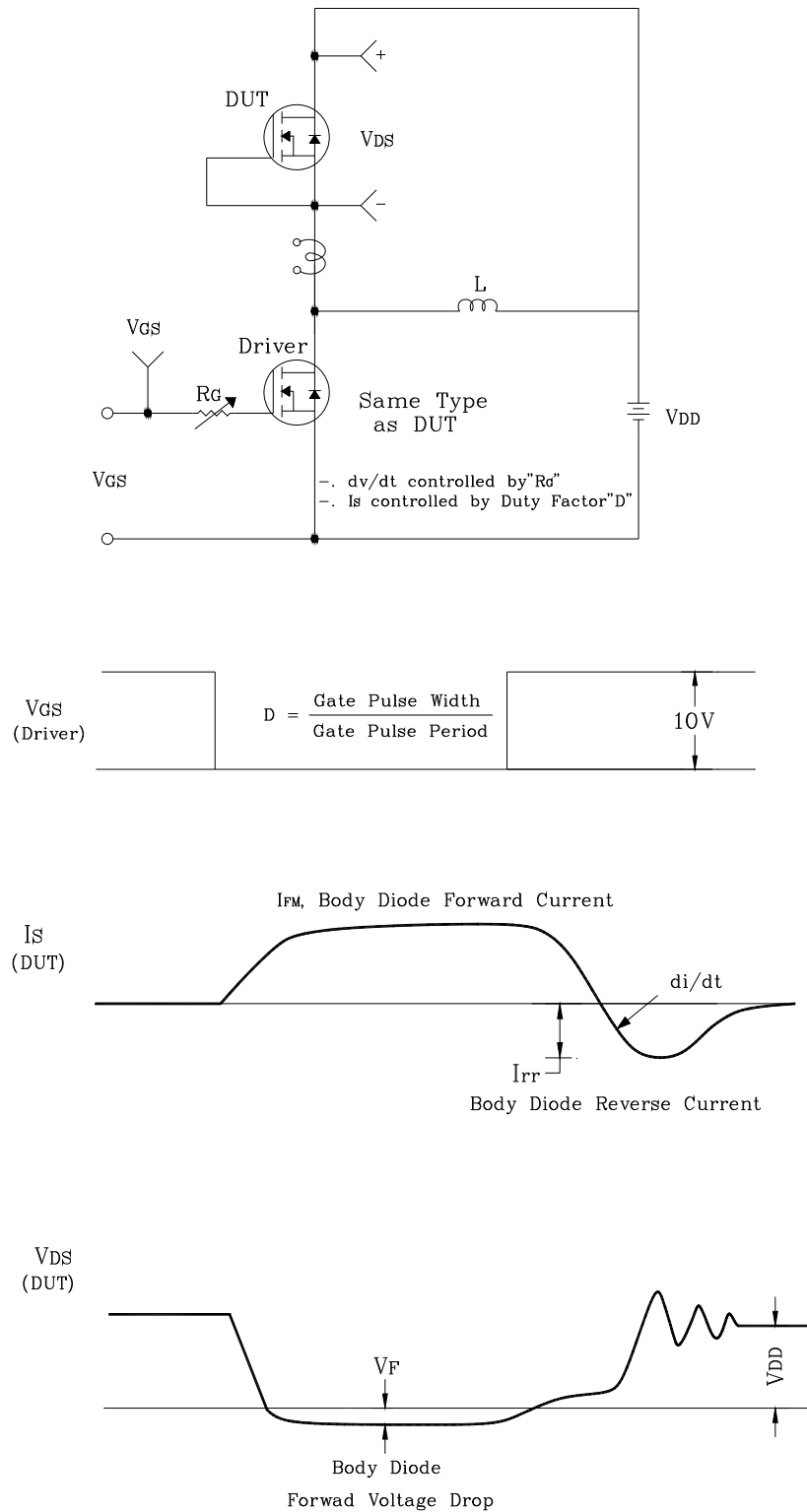
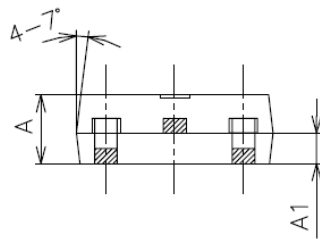
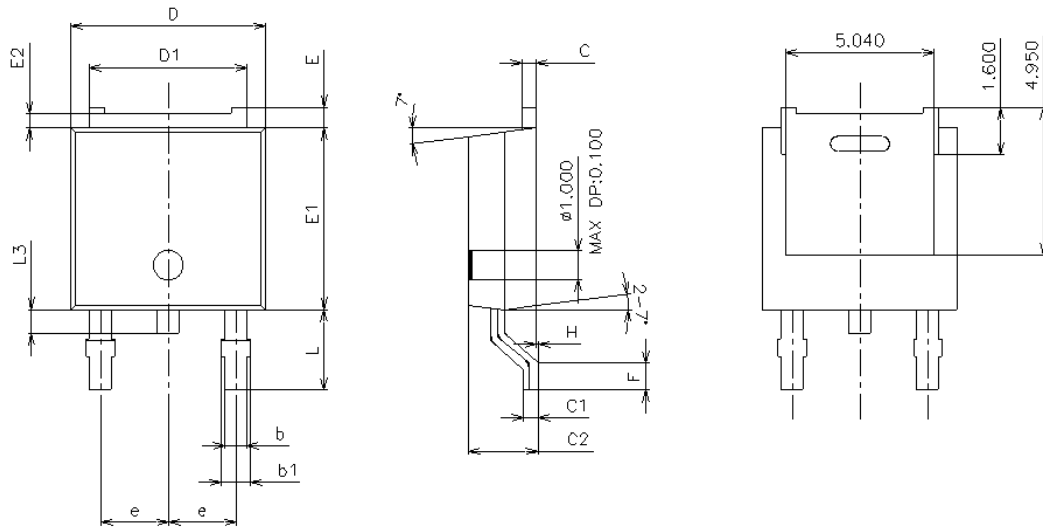


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

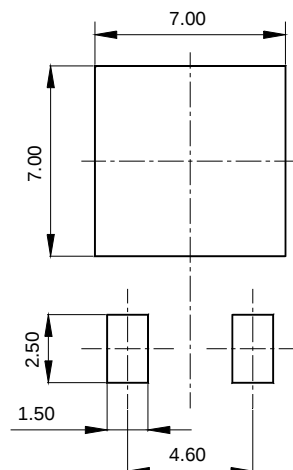


Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
D	6.40	6.60	6.80	
D1	5.14	5.34	5.54	
E	0.50	0.70	0.90	
E1	5.90	6.10	6.30	
E2	0.50 TYP			
A	2.20	2.30	2.40	
A1	0.87	1.07	1.27	
C	0.40	0.50	0.60	
C1	0.40	0.50	0.60	
C2	2.10	2.30	2.50	
L	2.50	2.70	2.90	
L3	0.60	0.80	1.00	
b	0.66	0.76	0.86	
b1	0.96 MAX			
e	2.10	2.30	2.50	
F	0.80 MIN			
H	0.00	-	0.10	

Recommended Land Pattern [unit: mm]



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