



# FQP12N60C

## N-Channel QFET<sup>®</sup> MOSFET

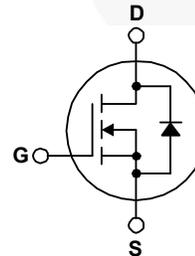
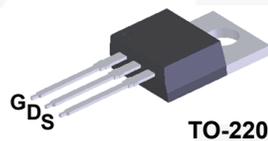
### 600 V, 12 A, 650 mΩ

#### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.

#### Features

- 12 A, 600 V,  $R_{DS(on)} = 650 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 6 \text{ A}$
- Low Gate Charge (Typ. 48 nC)
- Low Crss (Typ. 21 pF)
- 100% Avalanche Tested



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQP12N60C	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	12
		- Continuous ( $T_C = 100^\circ\text{C}$ )	7.4
$I_{DM}$	Drain Current - Pulsed (Note 1)	48	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	870	mJ
$I_{AR}$	Avalanche Current (Note 1)	12	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	22.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	225	W
		- Derate above $25^\circ\text{C}$	1.78
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

#### Thermal Characteristics

Symbol	Parameter	FQP12N60C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.56	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP12N60C	FQP12N60C	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

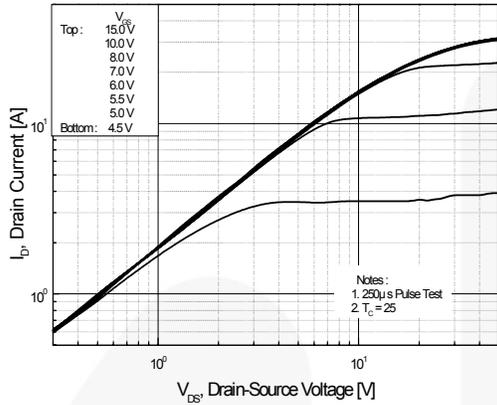
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA, T <sub>J</sub> = 25°C	600	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°	--	--	1 10	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6 A	--	0.53	0.65	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 6 A	--	13	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	1760	2290	pF
C <sub>oss</sub>	Output Capacitance		--	182	235	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	21	28	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 12 A R <sub>G</sub> = 25 Ω	--	30	70	ns
t <sub>r</sub>	Turn-On Rise Time		--	85	180	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	140	280	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	--	90	190
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 12 A V <sub>GS</sub> = 10 V	--	48	63	nC
Q <sub>gs</sub>	Gate-Source Charge		--	8.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4)	--	21	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	12	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	48	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 12 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 12 A di/dt = 100 A/μs	--	420	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	4.9	--	μC

### NOTES:

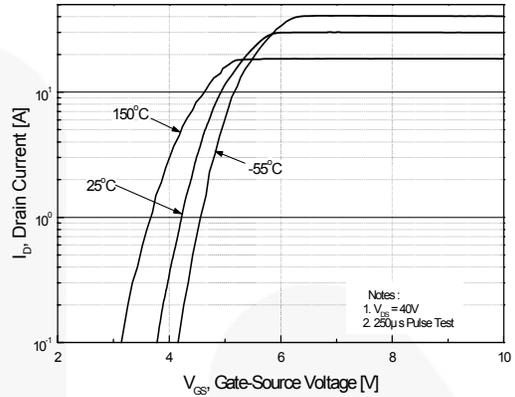
1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. L = 11 mH, I<sub>AS</sub> = 12 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 12 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

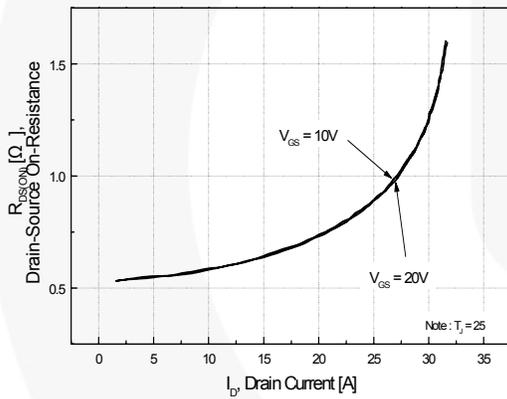
**Figure 1. On-Region Characteristics**



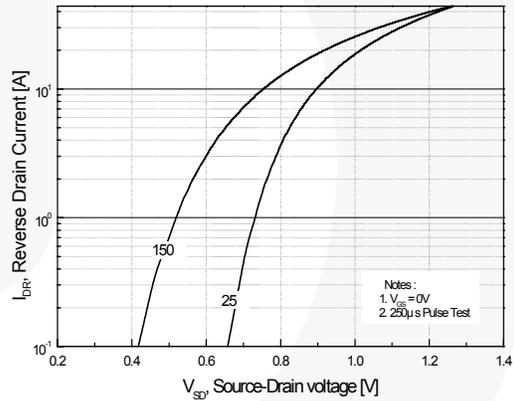
**Figure 2. Transfer Characteristics**



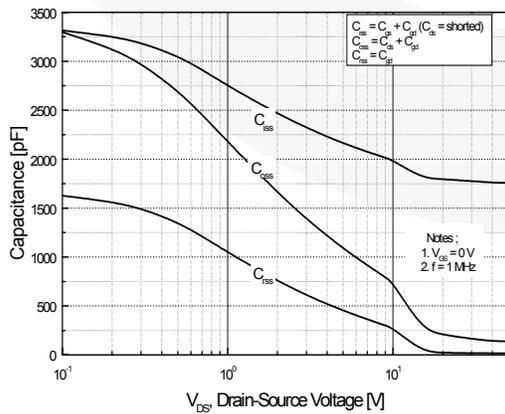
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



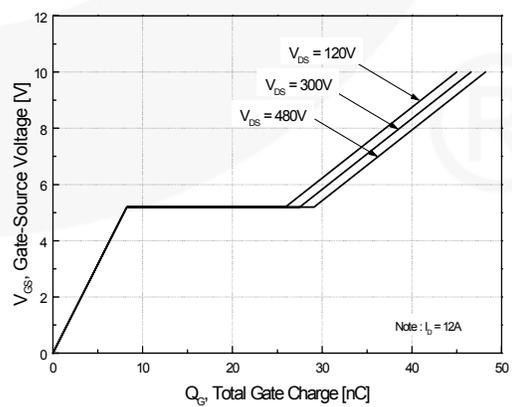
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

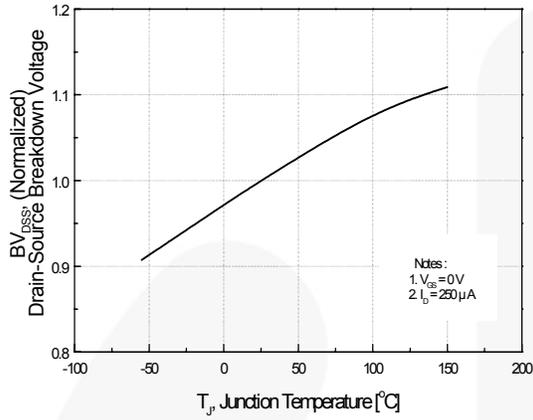


**Figure 6. Gate Charge Characteristics**

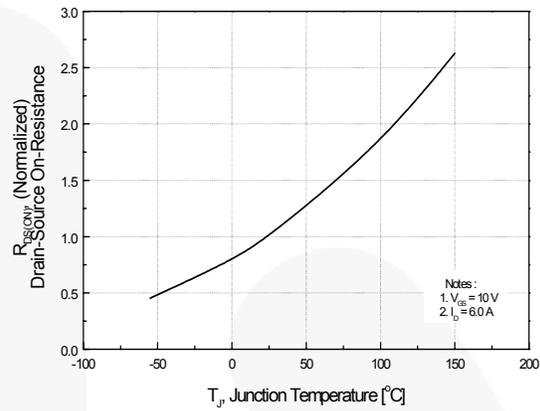


**Typical Performance Characteristics** (Continued)

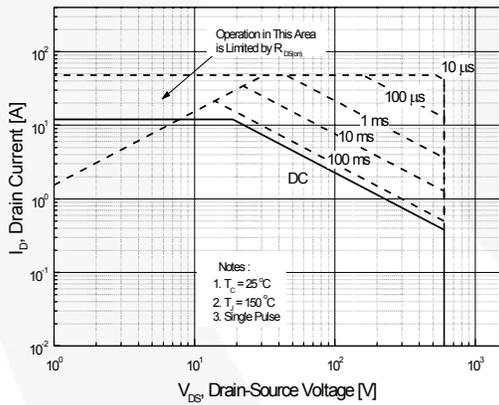
**Figure 7. Breakdown Voltage Variation vs. Temperature**



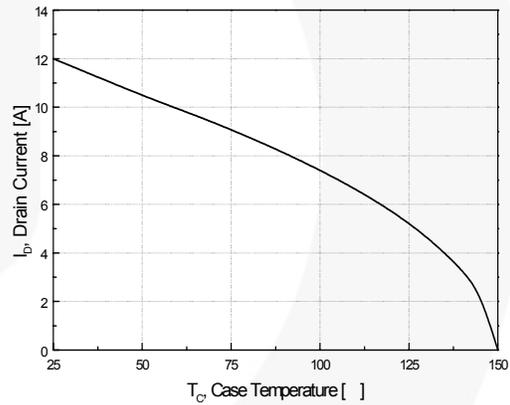
**Figure 8. On-Resistance Variation vs. Temperature**



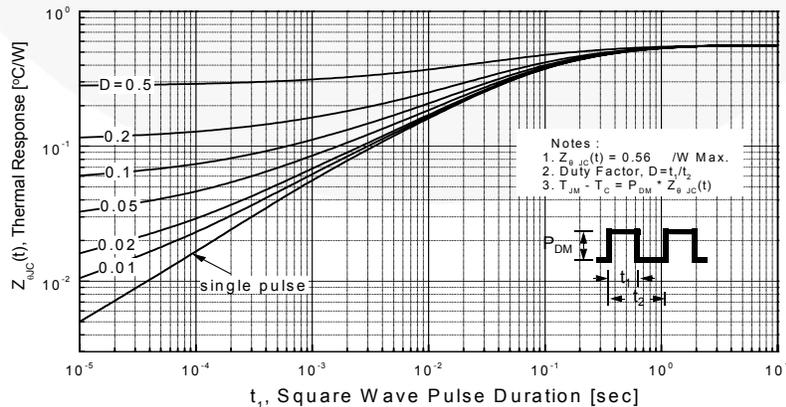
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**



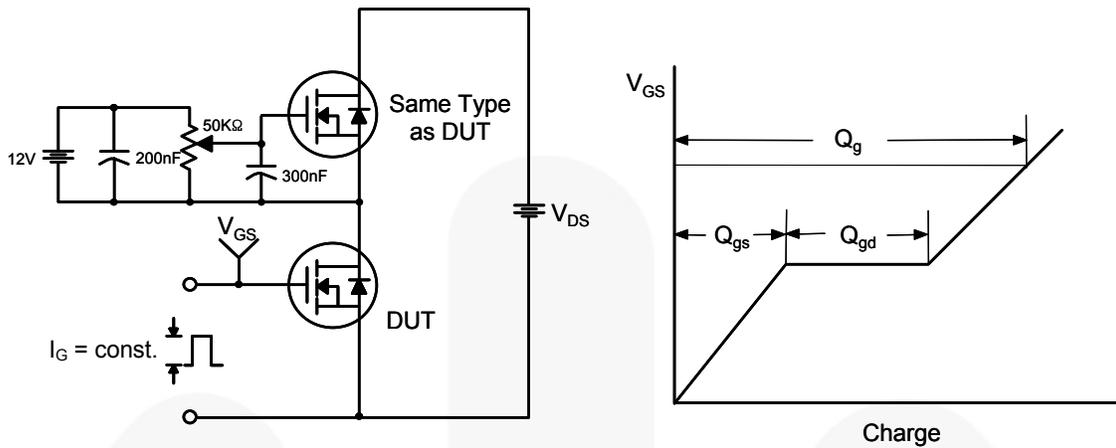


Figure 12. Gate Charge Test Circuit & Waveform

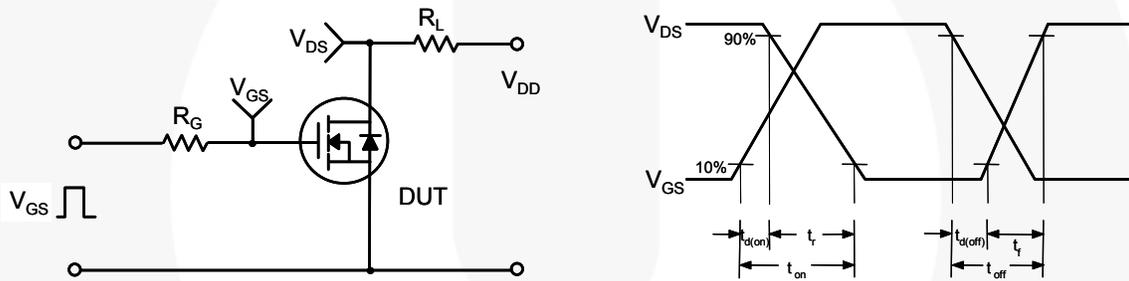


Figure 13. Resistive Switching Test Circuit & Waveforms

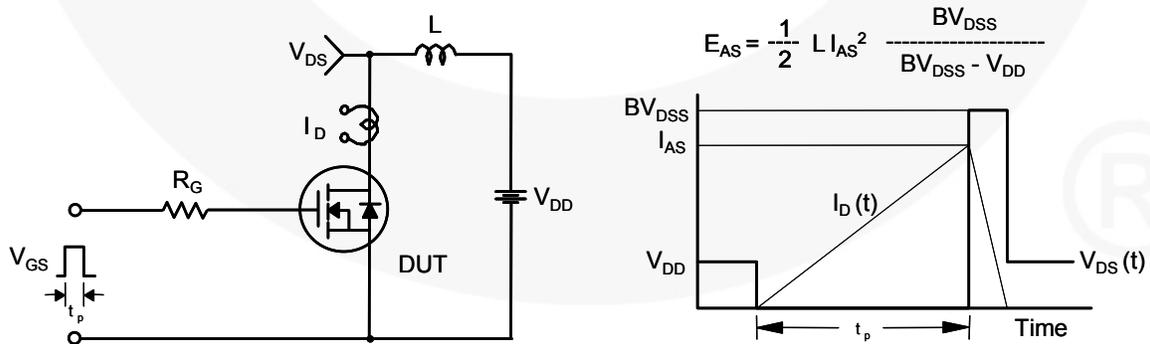


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

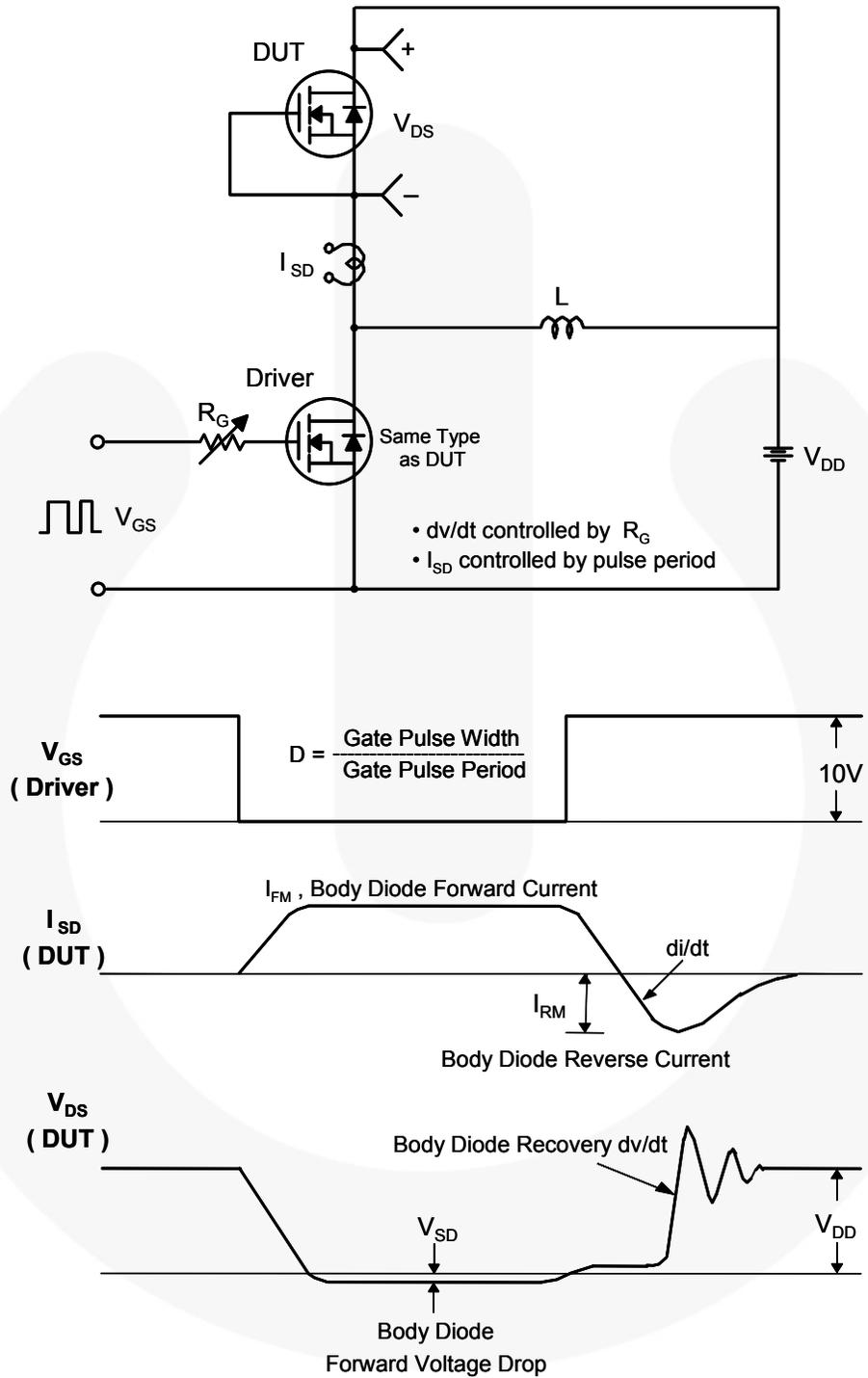
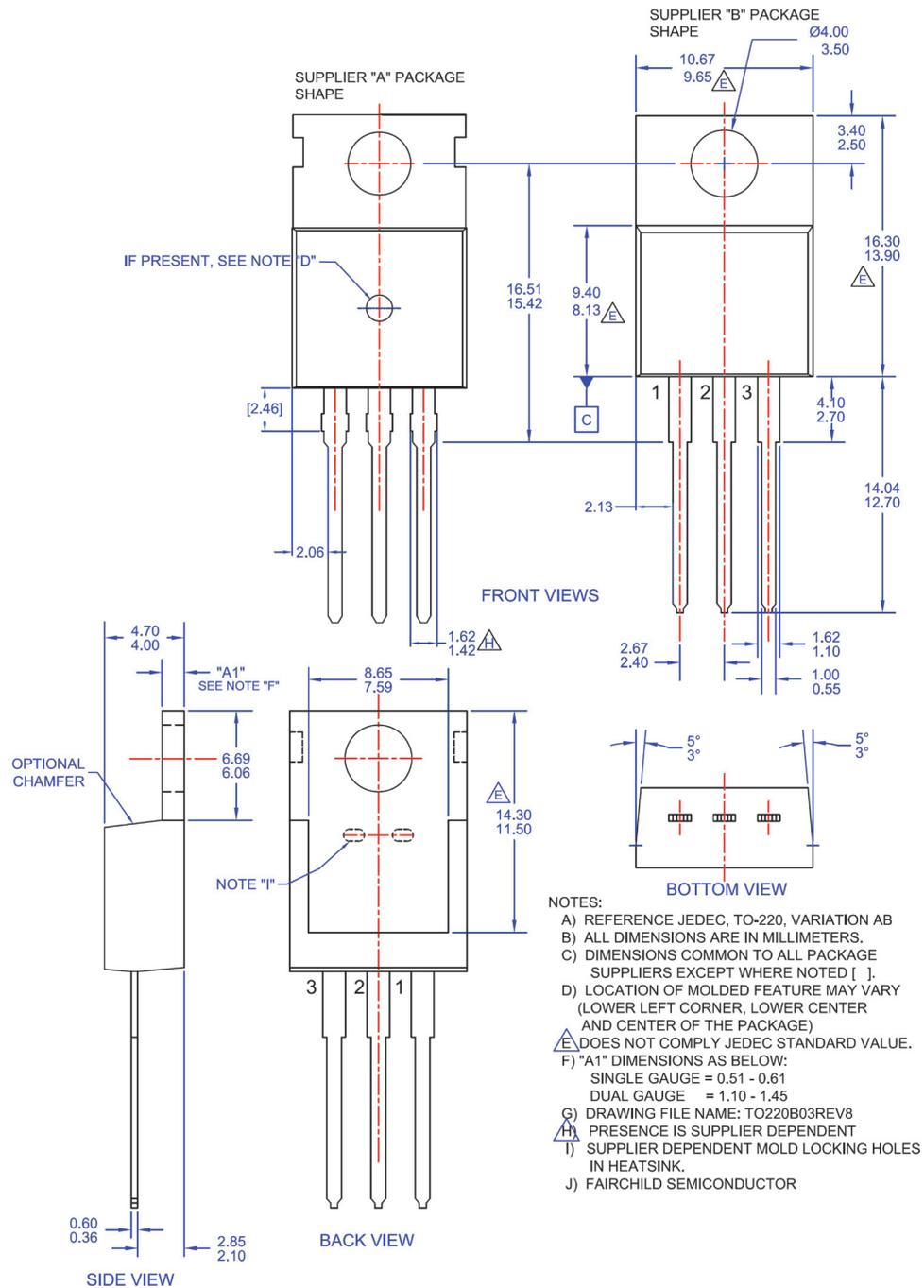


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO220, Molded, 3-Lead, Non Jedec Variation AB**

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